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DDR5 Clock Driver Definition (DDR5CKD01)

(From JEDEC Board Ballot JCB-23-55, formulated under the cognizance of the JC-40.4 sub-committee on Registered and Fully Buffered Memory Support Logic, item number 344.99D).

1 Scope

This document defines standard specifications of DC interface parameters, switching parameters, and test loading for definition of the DDR5 Clock Driver (CKD) for re-driving the DCK for CUDIMM, CSODIMM, and CAMM applications. The DDR5CKD01 Device ID is DID = 0x0531. (5 = DDR5, 3= Clock Driver, 1= rev 01)

The terms ‘DDR5CKD01, Clock Driver, ‘CKD’, or ‘device’ are used interchangeably to refer to this device in the remainder of this specification. Blue text is used to highlight Register Control words “RWxx” and font in some tables for ease of readability throughout the document.

The purpose is to provide a standard for the DDR5CKD01(see Note) logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

NOTE: The designation DDR5CKD01 refers to the part designation of a series of commercial logic parts common in the industry. This designation is normally preceded by a series of manufacturer specific characters to make up a complete part designation.

2 Mechanical Outline

Package options include a 35 -ball Fine-Pitch BGA (BGA) with 0.50 mm/0.50 mm ball pitch, 11 x4 grid. The package has a number of depopulated balls. Package size is 2.3 mm x 5.8 mm as defined in MO-276 Issue R, Variation PBGA-B29[36]_10p50-R2p3x4p8Z#-C0p375Z#[1].

The device pin out supports outputs on the top and outer left and right columns to support easy DIMM signal routing. Corresponding inputs are placed in a way to match the corresponding pin location on the connector and DIMM Standards.

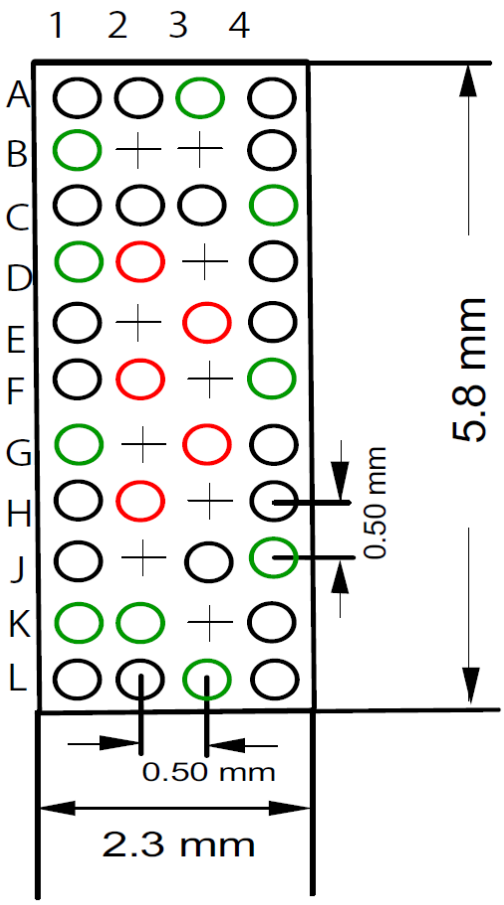


Figure 1 — Ball Configuration, TOP VIEW

Ball pitch: 0.50 mm x 0.50 mm, Size (ø 0.3 mm), SMD Pad SRO (ø 0.275 mm)
X-ray view from topside

1. This variation defines a maximum package thickness of 1.00 mm. The DDR5CKD01 must comply with a minimum thickness of 0.80 mm.

2.1 Pin Assignment

Table 1 specifies the pin assignment for the DDR5CKD01

Table 1 — Ball Assignment - TOP VIEW

	1	2	3	4	
A	DCK1_A_t	DCK1_A_c	VSS	DCK1_B_c	A
B	V_{SS}			DCK1_B_t	B
C	Z_{QCAL}	SDA	SCL	V_{SS}	C
D	V_{SS}	VDDIO		QCK1_B_c	D
E	QCK1_A_c		V_{DD}	QCK1_B_t	E
F	QCK1_A_t	V_{DD}		V_{SS}	F
G	V_{SS}		V_{DD}	QCK0_B_c	G
H	QCK0_A_c	V_{DD}		QCK0_B_t	H
J	QCK0_A_t		DRST_N	V_{SS}	J
K	V_{SS}	V_{SS}		DCK0_B_c	K
L	DCK0_A_t	DCK0_A_c	V_{SS}	DCK0_B_t	L
	1	2	3	4	

2.2 Terminal Functions

Table 2 — Terminal Functions

Signal Group	Signal Name	Type	Description	# of Pins
Clock Inputs	DCK0_A_t/DCK0_A_c DCK0_B_t/DCK0_B_c DCK1_A_t/DCK1_A_c DCK1_B_t/DCK1_B_c	POD differential	Differential Controller clock input pair.	8
Reset Input	DRST_n	CMOS input	Active LOW asynchronous reset input. When LOW, it causes a reset of the internal latches and disables the outputs, thereby forcing the outputs to float.	1
Outputs Clocks	QCK0_A_t/QCK0_A_c QCK1_A_t/QCK1_A_c QCK0_B_t/QCK0_B_c QCK1_B_t/QCK1_B_c	POD differential	Clock outputs to the DRAMs. Two copies per channel.	8
SidebandBus pins[1]	SDA	Open drain or push-pull I/O[2,3]	SidebandBus Data	1
	SCL	CMOS input[3]	SidebandBus Clock	1
	V_{DDIO}	Power input	SidebandBus power input	1
Miscellaneous pins	V_{DD}	Power Input	Power supply voltage	4
	V_{SS}	Ground Input	Ground	10
	ZQCAL	Reference	Reference pin for driver calibration	1
Total Number of Pins				35

NOTE 1 SA pins are not required for DDR5CKD01 as the address will be determined by the ZQ Resistor value.
NOTE 2 SDA driver operation is dynamic. Depending on the SidebandBus mode of operation I2C or I3C, and even on the specific step (byte or bit) of a SidebandBus transaction packet, the SDA output driver can operate either in open-drain mode or push-pull mode.
NOTE 3 These inputs are 0.9 to 2.1-V inputs.

Clock Naming Convention:

Input Example:
DCKx_N - where ‘x’ is the input clock rank number, and ‘N’ is the sub-channel.

Output Example:
QCKy_N - where ‘y’ is the rank number, and ‘N’ is the sub-channel.

3 Description

The DDR5CKD01 is a registering clock driver used on DDR5 CUDIMMs, CSODIMMs, and CAMM. Its primary function is to buffer the DDR clock between the host controller and the DRAMs.

3.1 Logic Diagram Positive Logic

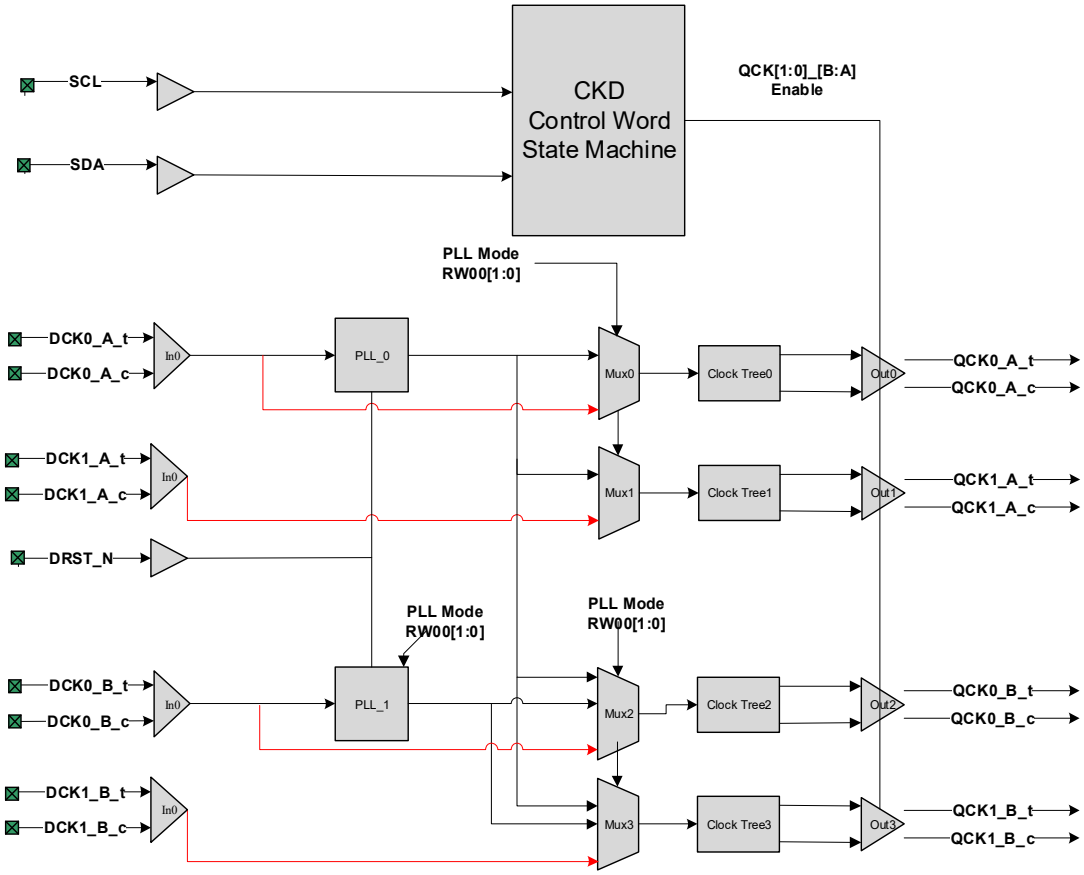


Figure 2 — Logic Diagram Positive Logic

4 Operation

4.1 CKD PLL Modes

The CKD has three clock driving modes, Single PLL Mode, PLL Bypass Mode (Legacy mode), and Dual PLL mode to generate the four output clock pairs QCK[1:0]_[B:A]_t/c.

The Host must write RW00[1:0] after V_{DD} has ramped and before driving any DCK clock pairs to configure the PLL mode when the device is in single or dual PLL mode.

In any of the PLL modes, the output clock frequency shall match that of the input clock in the frequency range of 1000 MHz to 4200 MHz.

Table 3 — Clock Mapping

RW00[1:0]	PLL Mode	PLL	Input Clock	Output Clock	Sub Channel
‘00’b	PLL Bypass[1,2]	N/A	DCK0_A_t/c	QCK0_A_t/c	A
			DCK1_A_t/c	QCK1_A_t/c	
			DCK0_B_t/c	QCK0_B_t/c	B
			DCK1_B_t/c	QCK1_B_t/c	
‘01’b	Single PLL[3]	PLL_0	DCK0_A_t/c	QCK0_A_t/c	A
				QCK1_A_t/c	
				QCK0_B_t/c	B
				QCK1_B_t/c	
‘10’b	Dual PLL[1,2,4]	PLL_0	DCK0_A_t/c	QCK0_A_t/c	A
				QCK1_A_t/c	
		PLL_1	DCK0_B_t/c	QCK0_B_t/c	B
				QCK1_B_t/c	

NOTE 1 When both DCK0_A and DCK0_B are toggling they cannot run at different frequencies.
NOTE 2 If one clock stops the other clock may continue to toggle within the normal frequency range.
NOTE 3 In Single PLL mode only PLL_0 is functional and PLL_1 is disabled to save power
NOTE 4 Both DCK0_A and DCK0_B must have a common reference clock and the SSC will be on the common reference clock. Due to the reference clock delay, the total DCK0_A and DCK0_B phase offset must be within t_{INCK_OFFSET}

4.1.1 PLL Bypass Mode

PLL Bypass mode normal operation is only supported for 990 MHz to 3000 MHz. Additionally, to support low speed ATE testing, PLL Bypass Mode will run below 990 MHz.

When RW00[1:0] = ’00’ PLL Bypass Mode is enabled, and the DCK[1:0]_[B:A]_t and DCK[1:0]_[B:A]_c are passed through to QCK[1:0]_[B:A]_t/c output clock pairs respectively. If only two output QCK pairs are required then QCK1_[B:A]_t/c can be disabled in RW00 to save power.

The delay from DCK to QCK is $t_{staoff_PLL_BYP}$ with $t_{dynoff_PLL_BYP}$ as the dynamic variation. When Host adjusts the phase of a DCK input clock pair, the phase of the corresponding QCK output clock pairs will be adjusted with the same offset.

In this mode, the input clock termination (ICT) resistors on DCK[1:0]_[B:A]_t/c are all connected to V_{SS} with programmable values.

4.1.2 Single PLL Mode

When RW00[1:0] = '01' the clock driver is in Single PLL Mode and the PLL_0 is enabled and the QCK[1:0]_[B:A]_t/c output clock pairs are re-generated by PLL_0 based on the DCK0_A_t/c input. PLL_1 is disabled. If only two QCK pairs are required, then QCK1_[B:A]_t/c can be disabled in RW00 to save power.

The delay from DCK0_A_t/c to QCK is t_{STAOFF} with t_{DYNOFF} as the dynamic variation. When Host adjusts the phase of the DCK0_A_t/c, the phase of all four QCK output pairs will be adjusted with the same offset.

In this mode, the input bus termination resistors on DCK0_A_t/c are all connected to V_{SS} with programmable values, and DCK1_A_t/c and DCK[1:0]_B_t/c are unused and terminated by the CKD ICT setting.

4.1.3 Dual PLL Mode

When RW00[1:0] = '10' the clock driver is in Dual PLL Mode and both PLL_0 and PLL_1 are enabled. The QCK[1:0]_[A]_t/c output clock pairs are re-generated by the PLL_0 based on the DCK0_A_t/c input and The QCK[1:0]_[B]_t/c output clock pairs are re-generated by the PLL_1 based on the DCK0_B_t/c input. If only two QCK pairs are required, then QCK1_[B:A]_t/c can be disabled in RW00 to save power.

The delay from DCK_t/c to QCK is t_{staoff} with t_{dynoff} as the dynamic variation. When Host adjusts the phase of the DCK0_A_t/c, the phase of QCK_A output pairs will be adjusted with the same offset. When Host adjusts the phase of the DCK0_B_t/c, the phase of QCK_B output pairs will be adjusted with the same offset.

In this mode, the input bus termination resistors on DCK0_[B:A]_t/c are all connected to V_{SS} with programmable values, and DCK1_[B:A]_t/c are unused and terminated by the CKD ICT setting.

4.2 Device Initialization

To ensure defined outputs from the CKD before a stable clock has been supplied, the CKD must enter the reset state during power-up. The CKD powers up with all control words at their default state. After the voltage ramp, stable power is provided for a minimum of t_{INIT1} with DRST_n asserted. When the reset input DRST_n is LOW, all input receivers are disabled. As long as the DRST_n input is pulled LOW, the CKD is in low power state and input termination is still enabled.

When DRST_n goes HIGH, the CKD will become operational after t_{CKDOP} regardless if input clock is toggling or not. After t_{STAB}, the device is in normal operating condition for Single and Dual PLL modes. When in PLL Bypass mode, the device will be in normal operation after the last $t_{staoff_PLL_BYP}$ is met.

After initialization, the Host must write to those control registers whose contents are required for the DIMM operation.

The DDR5CKD01 device will not affect DRST_n signal voltage levels even when V_{DD} is not powered on. A CKD with V_{DD} powered off shall not prevent other devices connected to the same DRST_n net from receiving the correct HIGH and LOW logic voltage levels driven by the host on that net. Also, the CKD device will not sustain permanent damage if DRST_n is driven HIGH (to V_{IH} levels) when V_{DD} is powered off, and it must be able to support all the specified features and functions once power is restored.

4.2.1 PLL Bypass Mode Initialization Sequence in PLL Bypass Mode

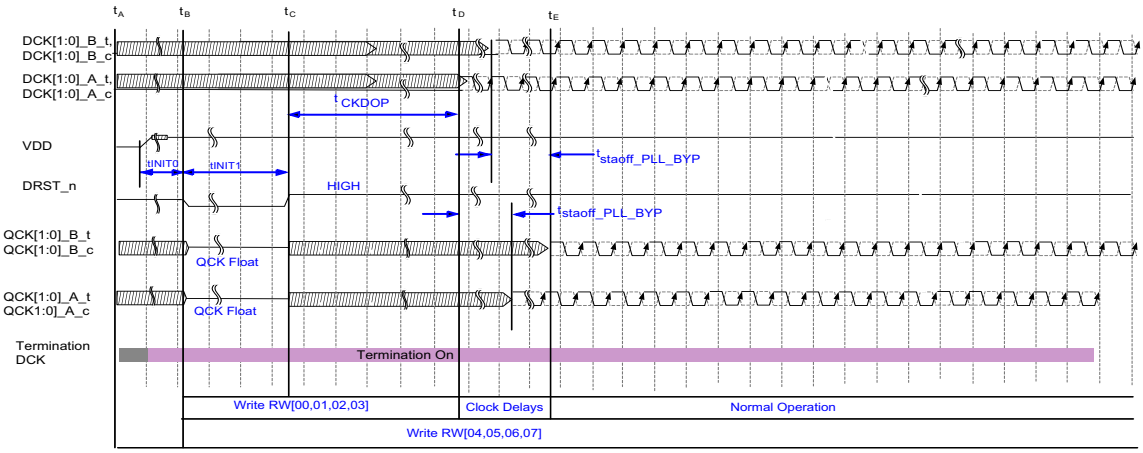


Figure 3 — Timing of Clock During Initialization Sequence in PLL Bypass Mode

NOTE 1 The host may write RW00[1:0] to enable PLL Bypass mode prior to any DCK toggling.

NOTE 2 If the host writes RW00 control word it must do so first before any other configuration control words to ensure device is properly configured.

NOTE 3 The CKD will not be operational until after t_{CKDOP} regardless if any required DCK is toggling or not.

NOTE 4 QCK may toggle during t_{CKDOP} if any required DCK is toggling.

NOTE 5 In the diagram DCK[1:0]_A starts before DCK[1:0]_B, but either clock may start toggling first.

4.2.2 Single PLL Mode Initialization Sequence

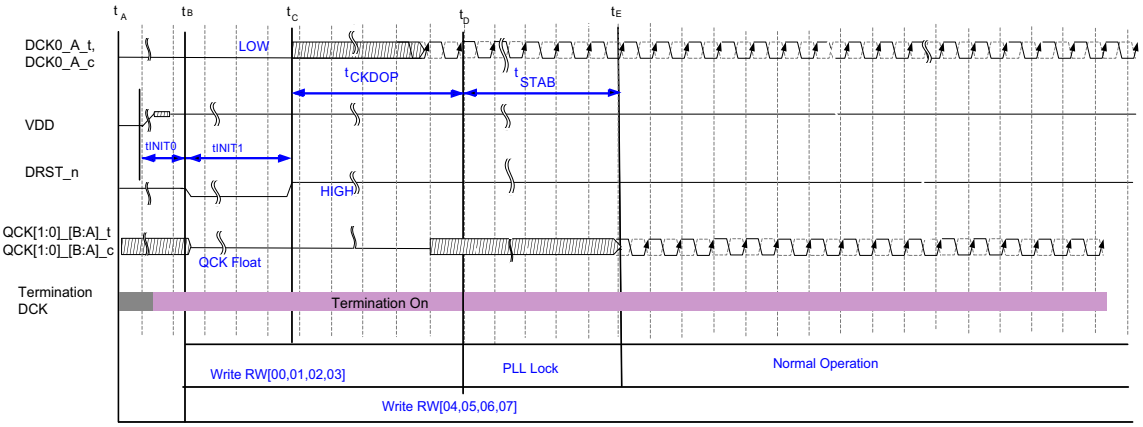


Figure 4 — Timing of Clock During Initialization Sequence in Single PLL Mode

NOTE 1 The host must write RW00[1:0] to enable Single PLL mode prior to DCK0_A toggling.

NOTE 2 The host must write RW00 before any other configuration control words.

NOTE 3 The CKD will not be operational until after t_{CKDOP} regardless if input DCK0_A is toggling.

NOTE 4 QCK may toggle during t_{CKDOP} if DCK0_A is toggling.

NOTE 5 The output clocks must be stable by the next DCK0_A rising edge after t_{STAB} max.

NOTE 6 During t_{STAB} while the PLL is locking, QCK output states are “Don’t Care”.

4.2.3 Dual PLL Mode Initialization Sequence

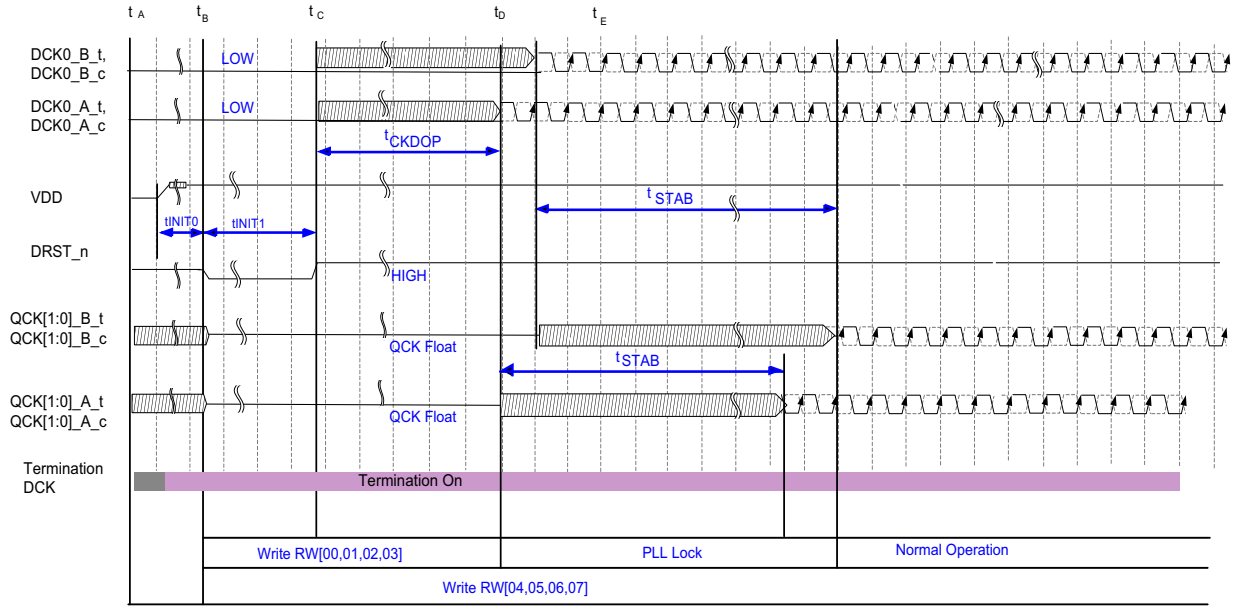


Figure 5 — Timing of Clock During Initialization Sequence in Dual PLL Mode

NOTE 1 The host must write RW00[1:0] to enable Dual PLL mode prior to DCK0_[B:A] toggling.

NOTE 2 The host must write RW00 before any other configuration control words.

NOTE 3 The CKD will not be operational until after t_{CKDOP} regardless if input DCK0_[B:A] is toggling.

NOTE 4 QCK may toggle during t_{CKDOP} if DCK0_[B:A] is toggling.

NOTE 5 The output clocks must be stable by the next DCK0_[B:A] rising edge after t_{STAB} max.

NOTE 6 During t_{STAB} while the PLL is locking, QCK output states are “Don’t Care”.

NOTE 7 In the diagram DCK0_A starts before DCK0_B, but either clock may start toggling first.

4.3 Reset Initialization with Stable Power

Applies to the situation when there is a soft reset in the system. All Control words are sticky cleared by power cycle not Reset.

4.3.1 PLL Bypass Mode Reset Initialization with Stable Power

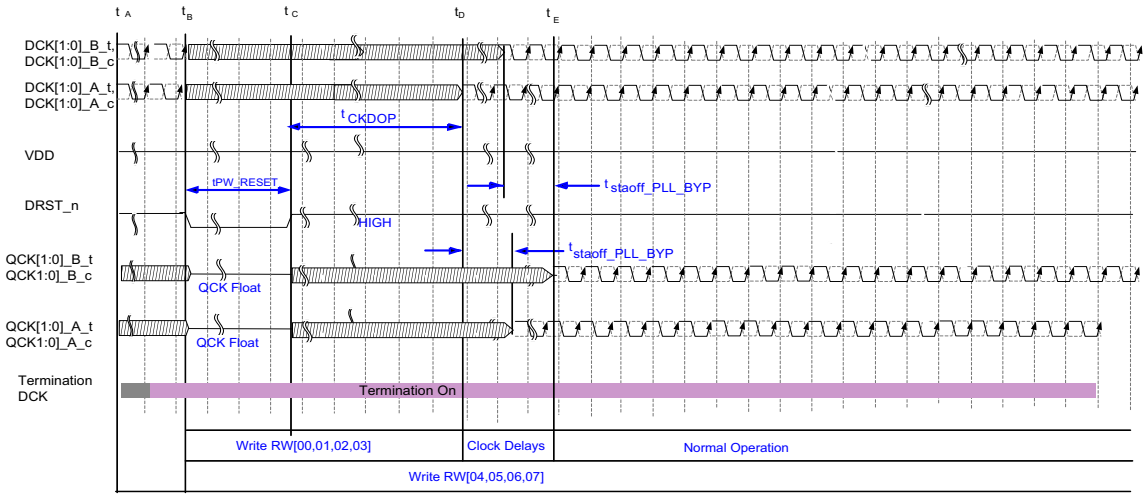


Figure 6 — Reset Initialization With Stable Power in PLL Bypass Mode.

NOTE 1 The CKD will not be operational until after t_{CKDOP} regardless if any required DCK is toggling.

NOTE 2 QCK may toggle during t_{CKDOP} if any required DCK is toggling.

NOTE 3 In the diagram DCK[1:0]_A start before DCK[1:0]_B, but any DCK clock pair may start toggling first.

4.3.2 Single PLL Mode Reset Initialization with Stable Power

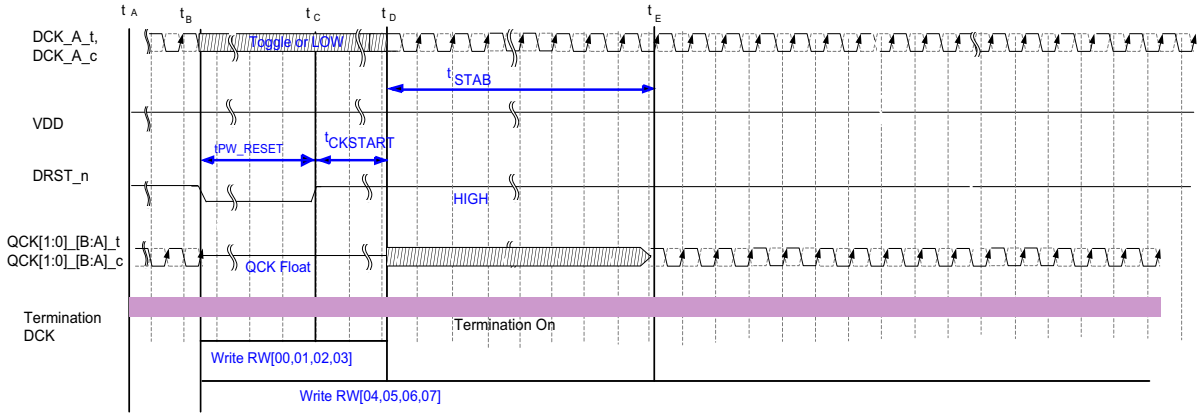


Figure 7 — Reset Initialization with Stable Power in Single PLL Mode

NOTE 1 If DCK is toggling QCK can start to toggle after DRST_n is de-asserted.

NOTE 2 The CKD will not be operational until after t_{CKDOP} regardless if input DCK0_A is toggling.

NOTE 3 QCK may toggle during t_{CKDOP} if DCK0_A is toggling.

NOTE 4 The output clocks must be stable by the next DCK0_A rising edge after t_{STAB} max.

NOTE 5 During t_{STAB} while the PLL is locking, QCK output states are “Don’t Care”.

4.3.3 Dual PLL Mode Reset Initialization with Stable Power

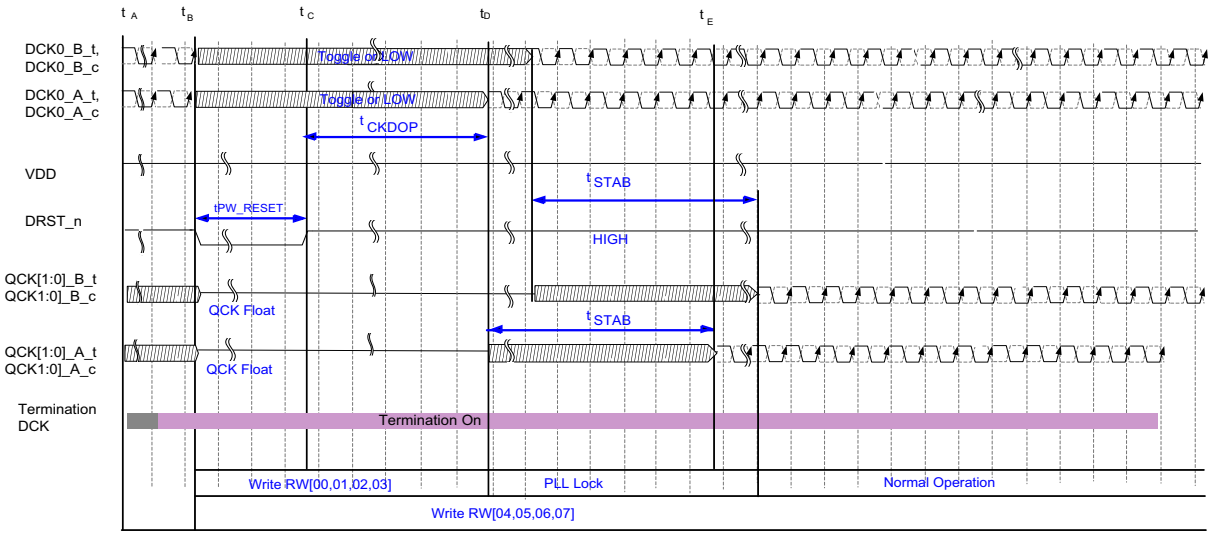


Figure 8 — Reset Initialization With Stable Power in Dual PLL Mode.

NOTE 1 If DCK0_[B:A] is toggling QCK can start to toggle after DRST_n is de-asserted.

NOTE 2 The CKD will not be operational until after t_{CKDOP} regardless if input DCK0_[B:A] is toggling.

NOTE 3 QCK may toggle during t_{CKDOP} if DCK0_[B:A] are toggling.

NOTE 4 The output clocks must be stable by the next DCK0_[B:A] rising edge after t_{STAB} max.

NOTE 5 During t_{STAB} while the PLL is locking, QCK output states are “Don’t Care”.

NOTE 6 In the diagram DCK0_A starts before DCK0_B, but either clock may start toggling first.

4.4 Clock Stop Operation

To support S3 Power Management mode or any other operation that allows output clocks to float, the CKD supports a Clock Stopped power down mode for Single and Dual PLL Modes. When inputs DCK_t and DCK_c are being held LOW for at least t_{DLOW} Min the device stops PLL operation and enters low-power static standby operation but Sideband Bus must be operational.

4.4.1 PLL Bypass Mode Clock Stopped Event

When the CKD is in PLL Bypass mode, it will remain in high powered state during clock stop event.

Note: Each Clock path works independently, input to corresponding output.

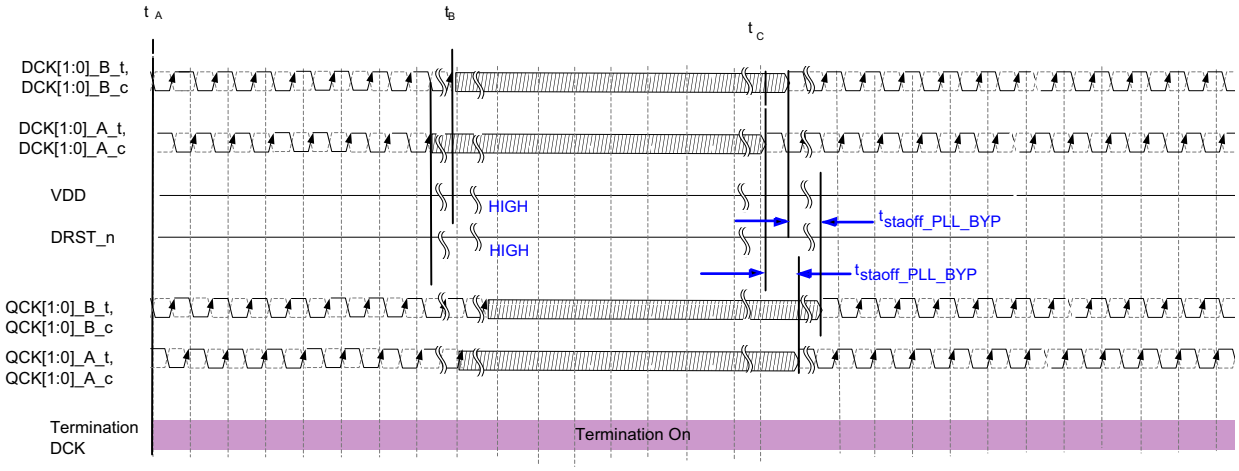


Figure 9 — PLL Bypass Mode during Clock Stop Event

4.4.2 Single PLL Mode Clock Stop Power Down

To enter Clock Stopped Power Down mode the host will stop driving (float) DCK0_A_t and DCK0_A_c. Since DCK is ODT terminated to V_{SS} the CKD receiver will see both DCK0_A_t and DCK0_A_c at a logic LOW below $V_{ilStatic_DC}$. This condition should be interpreted as clock stop power-down mode.To avoid clock glitches during clock power down, the V_{SS} termination on DCK_t/ DCK_c signals will pull the input clock signals below $V_{ILStatic}$ threshold.The CKD is now in Clock Stopped Power Down mode. The DCK0_A_t and DCK0_A_c remain active input circuits which are required to detect the wake up request from the host.

To Exit clock stop power down, a frequency and phase accurate input clock signal must be applied. The output clocks must be stable by the next DCK0 rising edge after t_{STAB} max.

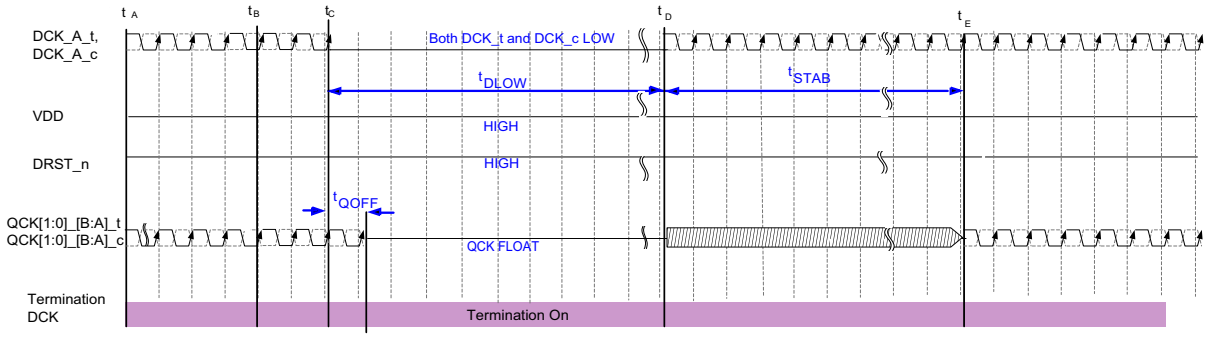


Figure 10 — Single PLL Mode Clock Stop Power Down

NOTE 1 During t_{STAB} while the PLL is locking, QCK output states are "Don't Care".

NOTE 2 The output clocks must be stable by the next DCK0_A rising edge after t_{STAB} max.

4.4.3 Dual PLL Mode Clock Stop Power Down

To enter CKD Clock Stopped Power Down mode, the host will stop driving (float) DCK0_[B:A]_t and DCK0_[B:A]_c. Since DCK is ODT terminated to V_{SS} the CKD receiver will see both input clock pairs DCK0_[B:A]_t and DCK0_[B:A]_c at a logic LOW. This condition should be interpreted as clock stop power-down mode.To avoid clock glitches during clock power down, the V_{SS} termination on DCK0_[B:A]_t/ DCK0_[B:A]_c signals will pull the input clock signals below $V_{ILStatic}$ threshold.The CKD is now in Clock Stopped Power Down mode. The DCK0_[B:A]_t and DCK0_[B:A]_c remain active input circuits which are required to detect the wake up request from the host.

To Exit clock stop power down wake up the CKD after entering Clock Stopped Power Down, a frequency and phase accurate input clock signal must be applied to either DCK0_A or DCK0_B. The output clocks must be stable by the next DCK rising edge after t_{STAB} max.

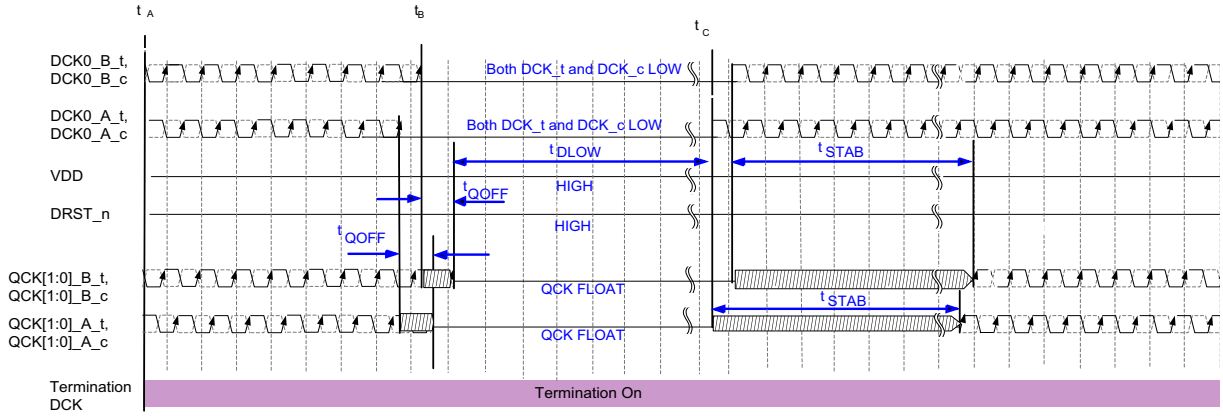


Figure 11 — Dual PLL Mode Clock Stop Power Down

NOTE 1 During t_{STAB} while the PLL is locking, QCK output states are “Don’t Care”.

4.5 Frequency Change

4.5.1 PLL Bypass Mode Frequency Change

The host can change input frequency if desired after a Clock Stop event. Once the host changes the frequency on the input DCK clocks the CKD will be required to drive stable output QCK clocks within $t_{staoff_PLL_BYP}$.

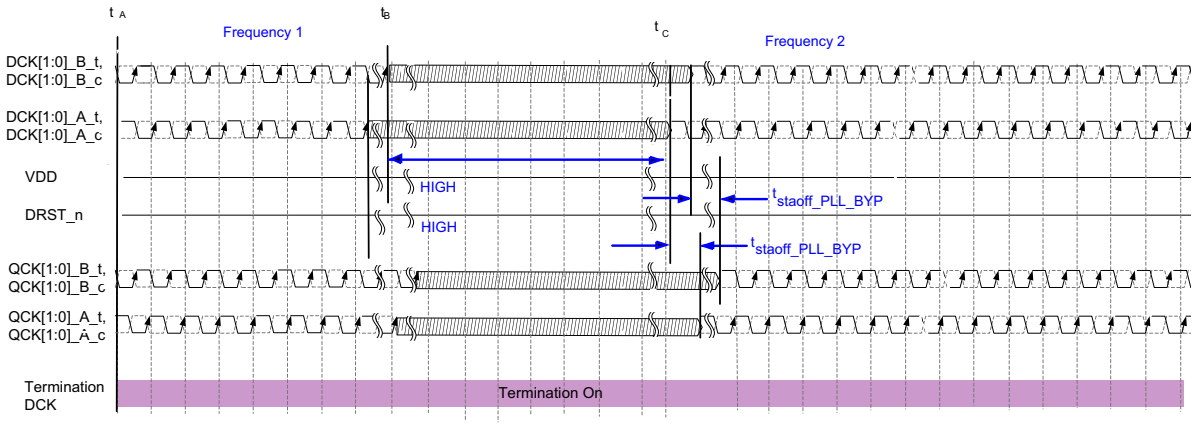


Figure 12 — Stabilization Time for Frequency Change for PLL Bypass Mode

4.5.2 Single PLL Mode Frequency Change

The host can change input frequency if desired after a Clock Stop Power Down event. Once the host changes the frequency on the in coming DCK clock, the CKD will re-lock to new frequency and will be required to drive a stable output clocks QCK within t_{STAB}.

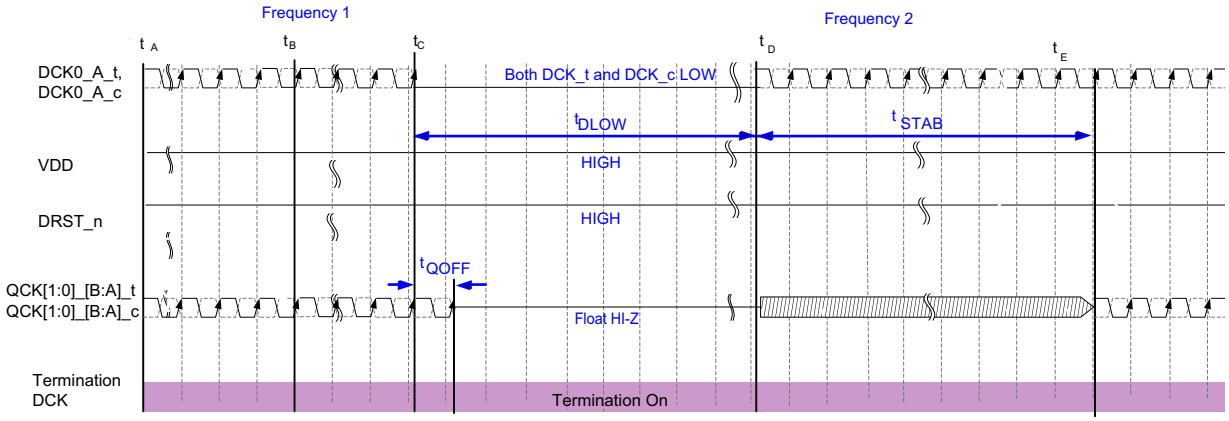


Figure 13 — Stabilization Time for Frequency Change for Single PLL Mode

NOTE 1 During t_{STAB} while the PLL is locking, QCK output states are "Don't Care".

4.5.3 Dual PLL Mode Frequency Change

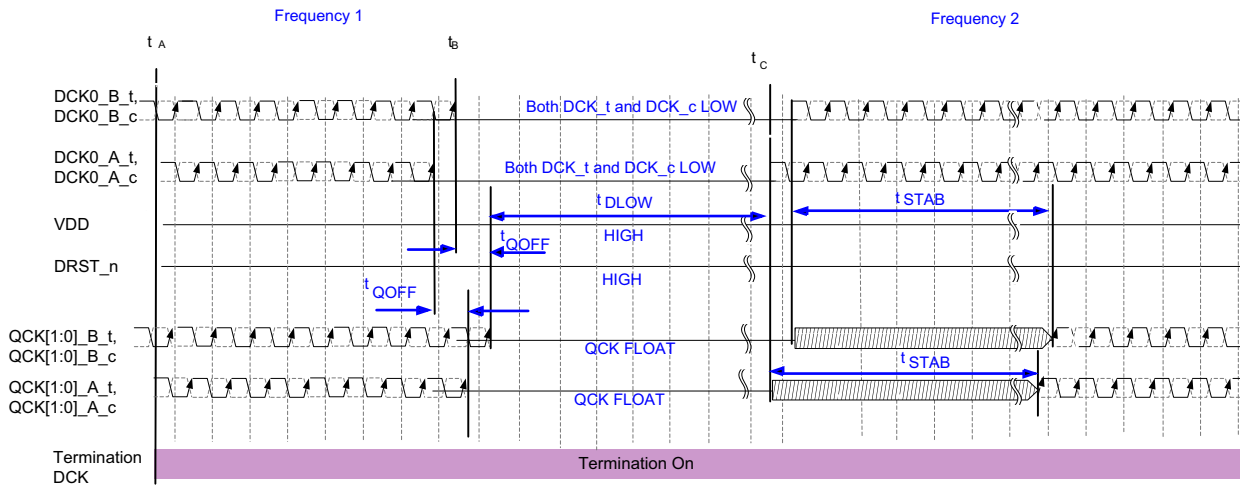


Figure 14 — Stabilization Time for Frequency Change for Dual PLL Mode

NOTE 1 During t_{STAB} while the PLL is locking, QCK output states are "Don't Care".

4.6 ZQ Calibration

ZQ Calibration calibrates the output driver and input termination impedance across process, temperature, and voltage. Since the CKD will not receive the ZQcal or ZQlatch commands the device will need to self-calibrate in the background while the clocks are continuously running. All specifications must be met during ZQCAL.

To use the ZQ calibration function, a 240 Ω or 480 Ω ± 1% tolerance external resistor must be connected between the ZQ pin and V_{SS}. For more details see Section 12.2.1, "Serial Address of CKD Device,"

4.7 Manufacturing ID

RW40 ~ RW4E are Read only control words in the DDR5CKD01 contain detailed CKD manufacturing information provided by CKD vendor. This information is programmed in OTP. The purpose is for improved manufacturing logistics management and not meant to be used by host platform to control normal operation. These registers must be accessible during run time.

4.8 Sideband

For all configuration registers, the DDR5CKD01 supports register control word access mechanisms through Sideband Bus Channel commands. The configuration registers are accessible to be written or read by software from the Sideband Bus host at any time the CKD is powered on, independent of input clock or reset. Details in Chapter 12, "Sideband Interface,".

5 Control Words

The DDR5CKD01 device features a set of 8-bit control words, which allow the optimization of the device properties for different raw card designs. The different control words and settings are described below. Any change to these control words require some time for the device to settle.

CKD Control Word attributes can be:

- Reserved[1]
- Read Only
- Write Only
- RD/WR
- One Time Programmable
- Sticky - Cleared by power cycle not Reset

5.1 Control Word Decoding

The power-on default state of all control words is ‘0’ unless specified otherwise. **All Control words are sticky cleared by power cycle not** DRST_n. Cycling the device in and out of low-power mode will not alter the control word settings.

Table 4 — CKD Control Word Space

Address	Size (bytes)	Space	Description
00h to 5Fh	96	JEDEC	96 addressed registers
60h to FFh	160	Vendor Specific	160 addressed registers

1. Reserved control bits may not be physically implemented and they shall be written to zero to ensure forward compatibility.

5.1.1 Control Word Decoding

Table 5 — Control Word Decoding

Register Control Word	MRA [7:0] HEX	Meaning
RW00	0x00	Configuration
RW01	0x01	Output Delay Control Enable
RW02	0x02	QCK Signals Driver Characteristics
RW03	0x03	QCK Output Differential Slew Rate
RW04	0x04	Output Delay Range for QCK0_A_t and QCK0_A_c
RW05	0x05	Output Delay Range for QCK1_A_t and QCK1_A_c
RW06	0x06	Output Delay Range for QCK0_B_t and QCK0_B_c
RW07	0x07	Output Delay Range for QCK1_B_t and QCK1_B_c
RW08	0x08	Reserved
RW09 -RW27	0x09 - 0x27	Reserved
RW28	0x28	I^2C and I3C Basic Error Status
RW29	0x29	I^2C and I3C Basic Clear Error Status
RW2A-RW3F	0x2A-0x3F	Reserved
RW40	0x40	Date Code Byte 0
RW41	0x41	Date Code Byte 1
RW42	0x42	Date Code Byte 2
RW43	0x43	Vendor Specific Unique Unit Code Byte 0
RW44	0x44	Vendor Specific Unique Unit Code Byte 1
RW45	0x45	Vendor Specific Unique Unit Code Byte 2
RW46	0x46	Vendor Specific Unique Unit Code Byte 3
RW47	0x47	Vendor Specific Unique Unit Code Byte 4
RW48	0x48	Vendor Specific Unique Unit Code Byte 5
RW49	0x49	Vendor Specific Unique Unit Code Byte 6
RW4A	0x4A	Vendor ID Byte 0
RW4B	0x4B	Vendor ID Byte 1
RW4C	0x4C	Device ID Byte 0
RW4D	0x4D	Device ID Byte 1
RW4E	0x4E	Vendor Revision ID
RW4F~RW5F	0x4F~0x5F	Reserved

Control Word Naming Convention:

RWyy[z:z]
yy = RW Number
z = OP

5.2 Configuration Control Word

5.2.1 RW00 - CKD Configuration Control Word

Table 6 — RW00: CKD Configuration Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	0	0	PLL Mode	Bypass Mode (default)
x	x	x	x	x	x	0	1		Single PLL mode[1]
x	x	x	x	x	x	1	0		Dual PLL mode
x	x	x	x	x	x	1	1		Reserved
x	x	x	x	0	0	x	x	ICT Input Clock Termination Settings	80 Ω (default)
x	x	x	x	0	1	x	x		60 Ω
x	x	x	x	1	0	x	x		120 Ω
x	x	x	x	1	1	x	x		Disabled[2]
x	x	x	0	x	x	x	x	CHA	QCK0_A_t/QCK0_A_c clock enabled
x	x	x	1	x	x	x	x	Disable QCK0_A_t/QCK0_A_c clock[3]	QCK0_A_t/QCK0_A_c clock disabled
x	x	0	x	x	x	x	x	CHA	QCK1_A_t/QCK1_A_c clock enabled
x	x	1	x	x	x	x	x	Disable QCK1_A_t/QCK1_A_c clock[3]	QCK1_A_t/QCK1_A_c clock disabled
x	0	x	x	x	x	x	x	CHB	QCK0_B_t/QCK0_B_c clock enabled
x	1	x	x	x	x	x	x	Disable QCK0_B_t/QCK0_B_c clock[3]	QCK0_B_t/QCK0_B_c clock disabled
0	x	x	x	x	x	x	x	CHB	QCK1_B_t/QCK1_B_c clock enabled
1	x	x	x	x	x	x	x	Disable QCK1_B_t/QCK1_B_c clock[3]	QCK1_B_t/QCK1_B_c clock disabled

NOTE 1 Only PLL0 is functional and PLL_1 is disabled to save power.

NOTE 2 This is for Testing purpose only.

NOTE 3 Output clocks may be individually turned on or off to conserve power. The system must read the module SPD to determine which clock outputs are used by the module. In PLL mode, the PLL remains locked on DCK0_t/DCK0_c unless the system stops the clock inputs to the DDR5CKD01 to enter the lowest power mode.

5.3 QCK Output Register Control Words

5.3.1 RW01- Output Delay Control Enable Control Word

Table 7 — RW01: Output Delay Control Enable Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	CHA QCK0_A_t/QCK0_A_c Output Delay	Disabled (zero delay)
x	x	x	x	x	x	x	1		Enabled[1]
x	x	x	x	x	x	0	x	CHA QCK1_A_t/QCK1_A_c Output Delay	Disabled (zero delay)
x	x	x	x	x	x	1	x		Enabled[2]
x	x	x	x	x	0	x	x	CHB QCK0_B_t/QCK0_B_c Output Delay	Disabled (zero delay)
x	x	x	x	x	1	x	x		Enabled[3]
x	x	x	x	0	x	x	x	CHB QCK1_B_t/QCK1_B_c Output Delay	Disabled (zero delay)
x	x	x	x	1	x	x	x		Enabled[4]
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

NOTE 1 Only valid for PLL Mode, enabled output delay feature range defined in RW04
NOTE 2 Only valid for PLL Mode, enabled output delay feature range defined in RW05
NOTE 3 Only valid for PLL Mode, enabled output delay feature range defined in RW06
NOTE 4 Only valid for PLL Mode, enabled output delay feature range defined in RW07

For details on CKD output driver strengths in this section, see Table 46, “Output Ron Drive,”.

5.3.2 RW02 - QCK Signals Driver Characteristics Control Word

Table 8 — RW02: QCK Signals Driver Characteristics Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	0	0	CHA QCK0_A_t/QCK0_A_c	Light Drive (Default)
x	x	x	x	x	x	0	1		Moderate Drive
x	x	x	x	x	x	1	0		Strong Drive
x	x	x	x	x	x	1	1		Weak Drive
x	x	x	x	0	0	x	x	CHA QCK1_A_t/QCK1_A_c	Light Drive (Default)
x	x	x	x	0	1	x	x		Moderate Drive
x	x	x	x	1	0	x	x		Strong Drive
x	x	x	x	1	1	x	x		Weak Drive
x	x	0	0	x	x	x	x	CHB QCK0_B_t/QCK0_B_c	Light Drive (Default)
x	x	0	1	x	x	x	x		Moderate Drive
x	x	1	0	x	x	x	x		Strong Drive
x	x	1	1	x	x	x	x		Weak Drive
0	0	x	x	x	x	x	x	CHB QCK1_B_t/QCK1_B_c	Light Drive (Default)
0	1	x	x	x	x	x	x		Moderate Drive
1	0	x	x	x	x	x	x		Strong Drive
1	1	x	x	x	x	x	x		Weak Drive

5.3.3 RW03 - QCK Output Differential Slew Rate Control Word

The CKD will support output slew rate control per channel, as described in the following control word.

Table 9 — RW03 - QCK Output Differential Slew Rate Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	0	0	CHA QCK [1:0]_A Differential Slew Rate Setting[1]	Moderate
x	x	x	x	x	x	0	1		Fast
x	x	x	x	x	x	1	0		Reserved
x	x	x	x	x	x	1	1		Reserved
x	x	x	x	0	0	x	x	Reserved	Reserved
x	x	x	x	0	1	x	x		Reserved
x	x	x	x	1	0	x	x		Reserved
x	x	x	x	1	1	x	x		Reserved
x	x	0	0	x	x	x	x	CHB QCK [1:0]_B Differential Slew Rate Setting[1]	Moderate
x	x	0	1	x	x	x	x		Fast
x	x	1	0	x	x	x	x		Reserved
x	x	1	1	x	x	x	x		Reserved
0	0	x	x	x	x	x	x	Reserved	Reserved
0	1	x	x	x	x	x	x		Reserved
1	0	x	x	x	x	x	x		Reserved
1	1	x	x	x	x	x	x		Reserved

NOTE 1 Slew Rate Control encodings of Moderate, and Fast apply to all driver strength settings. The base range values specified in Table 44 are applicable for only Ron = Strong Drive, V_{DD} = 1.1 V, and 25 °C. Slew rates will be less for other Ron values. The Output slew rate is verified by design and characterization, and may not be subject to production test.

5.3.4 RW04 to RW07 - QCKn Output Delay Range Control Word

Table 10 — RW04 to RW07: QCKn Output Delay Range Control Word

Setting								Definition	Encoding[1]
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	0	0	0	0	0	QCKn output delay setting[2,3,4,5,6]	0 ps (default)
x	x	x	0	0	0	0	1		4 ps
x	x	x	0	0	0	1	0		8 ps
x	x	x	0	0	0	1	1		12 ps
x	x	x	0	0	1	0	0		16 ps
x	x	x	0	0	1	0	1		20 ps
x	x	x	0	0	1	1	0		24 ps
x	x	x	0	0	1	1	1		28 ps
x	x	x	0	1	0	0	0		32 ps
x	x	x	0	1	0	0	1		36 ps
x	x	x	0	1	0	1	0		40 ps
x	x	x	0	1	0	1	1		44 ps
x	x	x	0	1	1	0	0		48 ps
x	x	x	0	1	1	0	1		52 ps
x	x	x	0	1	1	1	0		56 ps
x	x	x	0	1	1	1	1		60 ps
x	x	x	1	0	0	0	0		64 ps
x	x	x	1	0	0	0	1		68 ps
x	x	x	1	0	0	1	0		72 ps
x	x	x	1	0	0	1	1		76 ps
x	x	x	1	0	1	0	0		80 ps
x	x	x	1	0	1	0	1		84 ps
x	x	x	1	0	1	1	0		88 ps
x	x	x	1	0	1	1	1		92 ps
x	x	x	1	1	0	0	0		96 ps
x	x	x	1	1	0	0	1		Not Used
x	x	x	1	1	0	1	0		Not Used
x	x	x	1	1	0	1	1		Not Used
x	x	x	1	1	1	0	0		Not Used
x	x	x	1	1	1	0	1		Not Used
x	x	x	1	1	1	1	0		Not Used
x	x	x	1	1	1	1	1		Not Used
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

NOTE 1 Values are typical at PVT and not compensated

NOTE 2 This register is ignored in PLL Bypass Mode RW00[1:0] ='00'.

NOTE 3 When feature is enabled the delay settings require a time of t_{ODU} for the delay to become stable on the outputs.

NOTE 4 For any changes to RW04 to RW07, the jitter and duty cycle specs do not apply during tODU.

NOTE 5 Values can be changed while maintaining a constant output frequency.

NOTE 6 The allowed tolerance range of the delay is (-Max[20%, 1LSB], + Max[20%, 1LSB]) of the set delay value.

5.3.5 RW28: I²C and I3C Basic Error Status Word

Table 11 — RW28: I²C and I3C Basic Error Status Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	Error in Parity Check[1,2,3]	No PARITY error has been detected
x	x	x	x	x	x	x	1		PARITY error has been detected[4]
x	x	x	x	x	x	0	x	Error in Packet Error Code Check[1,2,5]	No PEC error has been detected
x	x	x	x	x	x	1	x		PEC error has been detected[6]
x	x	x	x	x	0	x	x	Reserved	Reserved
x	x	x	x	x	1	x	x		Reserved
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Device Event In-Band Interrupt Status[1]	No Pending IBI[7]
1	x	x	x	x	x	x	x		Pending IBI[8]

NOTE 1 This is a Read-Only Status bit. This is a Sticky register (not cleared by DRST_n).

NOTE 2 This register is automatically cleared to '0' when the Timeout Reset condition described in Section 13.2 is detected.

NOTE 3 This status bit only applies when I3C Basic mode is enabled or for CCC supported in I²C mode, provided that the Parity Checking function is not disabled.

NOTE 4 The CKD device detected a PARITY error in one or more bytes received.

NOTE 5 This status bit only applies when I3C Basic mode is enabled.

NOTE 6 The CKD device detected a PEC error for one or more data packets received. When a PEC error is detected in I²C mode, this status field will not be updated.

NOTE 7 The IBI status bit gets cleared to '0' when the CKD device processes a complete IBI operation (including uninterrupted IBI payload). This status bit also gets cleared when RW28[0] and RW28[1] become '00' after a Clear command in RW29.

NOTE 8 The IBI status bit gets set to '1' when the CKD sets RW28[0] or RW28[1] to '1' after detecting a Parity Error or a PEC Error.

5.3.6 RW29: I²C and I3C Basic Clear Error Status Word

Table 12 — RW29: I²C and I3C Basic Clear Error Status Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	Clear Parity Error Status[1]	No effect.
x	x	x	x	x	x	x	1		Clear RW28[0]
x	x	x	x	x	x	0	x	Clear Packet Error Status[1]	No effect.
x	x	x	x	x	x	1	x		Clear RW28[1]
x	x	x	x	x	0	x	x	Reserved	Reserved
x	x	x	x	x	1	x	x		Reserved
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

NOTE 1 This is a Write-1 Only register bit, and it self clears after the target status register has been cleared.

5.4 Manufacturing ID Control Words

5.4.1 RW40 - Date Code Byte 0 Word

Table 13 — RW40: Date Code Byte 0 Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	0	0	0	0	Date Code Digit 0[1,2] Year Information- Ones Digit (Read Only)	Digit = 0
x	x	x	x	0	0	0	1		Digit = 1
x	x	x	x	0	0	1	0		Digit = 2
x	x	x	x	...					...
x	x	x	x	0	1	1	1		Digit = 7
x	x	x	x	1	0	0	0		Digit = 8
x	x	x	x	1	0	0	1		Digit = 9
x	x	x	x	1	0	1	0		Codes 10 to 15 Reserved
x	x	x	x	...					
x	x	x	x	1	1	1	1		
0	0	0	0	x	x	x	x	Date Code Digit 1[1, 2] Year Information - Tens Digit (Read Only)	Digit = 0
0	0	0	1	x	x	x	x		Digit = 1
0	0	1	0	x	x	x	x		Digit = 2
...				x	x	x	x		...
0	1	1	1	x	x	x	x		Digit = 7
1	0	0	0	x	x	x	x		Digit = 8
1	0	0	1	x	x	x	x		Digit = 9
1	0	1	0	x	x	x	x		Codes 10 to 15 Reserved
...				x	x	x	x		
1	1	1	1	x	x	x	x		

NOTE 1 Programmed and locked in one time programmable memory by DDR5CKD01 vendor.

NOTE 2 This is year date code byte for CKD. It must be represented in Binary Coded Decimal (BCD). For example, year 2015 would be coded as 0x15 (0001 0101).

5.4.2 RW41 - Date Code Byte 1 Word

Table 14 — RW41: Date Code Byte 1 Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	0	0	0	0	Date Code Digit 2[1,2] Work Week Information - Ones Digit ISO 8601 compliant (Read Only)	Digit = 0
x	x	x	x	0	0	0	1		Digit = 1
x	x	x	x	0	0	1	0		Digit = 2
x	x	x	x	...					...
x	x	x	x	0	1	1	1		Digit = 7
x	x	x	x	1	0	0	0		Digit = 8
x	x	x	x	1	0	0	1		Digit = 9
x	x	x	x	1	0	1	0		Codes 10 to 15 Reserved
x	x	x	x	...					
x	x	x	x	1	1	1	1		
0	0	0	0	x	x	x	x	Date Code Digit 3[1, 2] Work Week Information- Tens Digit ISO 8601 compliant (Read Only)	Digit = 0
0	0	0	1	x	x	x	x		Digit = 1
0	0	1	0	x	x	x	x		Digit = 2
...				x	x	x	x		...
0	1	1	1	x	x	x	x		Digit = 7
1	0	0	0	x	x	x	x		Digit = 8
1	0	0	1	x	x	x	x		Digit = 9
1	0	1	0	x	x	x	x		Codes 10 to 15 Reserved
...				x	x	x	x		
1	1	1	1	x	x	x	x		

NOTE 1 Programmed and locked in one time programmable memory by DDR5CKD01 vendor.

NOTE 2 This is work week date code byte for RCD. It must be represented in Binary Coded Decimal (BCD). For example, week 47 would be coded as 0x47 (0100 0111).

5.4.3 RW42 - Date Code Byte 2 Word

Table 15 — RW42: Date Code Byte 2 Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	0	0	0	0	Date Code Digit 4[1] (Read Only)	Digit = 0
x	x	x	x	0	0	0	1		Digit = 1
x	x	x	x	0	0	1	0		Digit = 2
x	x	x	x	...					...
x	x	x	x	0	1	1	1		Digit = 7
x	x	x	x	1	0	0	0		Digit = 8
x	x	x	x	1	0	0	1		Digit = 9
x	x	x	x	1	0	1	0		Codes 10 to 15 Reserved
x	x	x	x	...					
x	x	x	x	1	1	1	1		
0	0	0	0	x	x	x	x	Date Code Digit 5[1] (Read Only)	Digit = 0
0	0	0	1	x	x	x	x		Digit = 1
0	0	1	0	x	x	x	x		Digit = 2
...				x	x	x	x		...
0	1	1	1	x	x	x	x		Digit = 7
1	0	0	0	x	x	x	x		Digit = 8
1	0	0	1	x	x	x	x		Digit = 9
1	0	1	0	x	x	x	x		Codes 10 to 15 Reserved
...				x	x	x	x		
1	1	1	1	x	x	x	x		

NOTE 1 Programmed and locked in one time programmable memory by DDR5CKD01 vendor.

5.4.4 RW43 - Vendor Specific Unique Unit Code Byte 0 Word

Table 16 — RW43: Vendor Specific Unique Unit Code Byte 0 Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	Byte 0 of Unique Unit Code[1] (Read Only)	Code 0
0	0	0	0	0	0	0	1		Code 1
0	0	0	0	0	0	1	0		Code 2
...									...
1	1	1	1	1	1	0	1		Code 253
1	1	1	1	1	1	1	0		Code 254
1	1	1	1	1	1	1	1		Code 255

NOTE 1 Programmed and locked in one time programmable memory by DDR5CKD01 vendor.

5.4.5 RW44 - Vendor Specific Unique Unit Code Byte 1 Word

Table 17 — RW44: Vendor Specific Unique Unit Code Byte 1 Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	Byte 1 of Unique Unit Code[1] (Read Only)	Code 0
0	0	0	0	0	0	0	1		Code 1
0	0	0	0	0	0	1	0		Code 2
...									...
1	1	1	1	1	1	0	1		Code 253
1	1	1	1	1	1	1	0		Code 254
1	1	1	1	1	1	1	1		Code 255

NOTE 1 Programmed and locked in one time programmable memory by DDR5CKD01 vendor.

5.4.6 RW45 - Vendor Specific Unique Unit Code Byte 2 Word

Table 18 — RW45: Vendor Specific Unique Unit Code Byte 2 Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	Byte 2 of Unique Unit Code[1] (Read Only)	Code 0
0	0	0	0	0	0	0	1		Code 1
0	0	0	0	0	0	1	0		Code 2
...									...
1	1	1	1	1	1	0	1		Code 253
1	1	1	1	1	1	1	0		Code 254
1	1	1	1	1	1	1	1		Code 255
NOTE 1 Programmed and locked in one time programmable memory by DDR5CKD01 vendor.									

5.4.7 RW46 - Vendor Specific Unique Unit Code Byte 3 Word

Table 19 — RW46: Vendor Specific Unique Unit Code Byte 3 Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	Byte 3 of Unique Unit Code[1] (Read Only)	Code 0
0	0	0	0	0	0	0	1		Code 1
0	0	0	0	0	0	1	0		Code 2
...									...
1	1	1	1	1	1	0	1		Code 253
1	1	1	1	1	1	1	0		Code 254
1	1	1	1	1	1	1	1		Code 255
NOTE 1 Programmed and locked in one time programmable memory by DDR5CKD01 vendor.									

5.4.8 RW47 - Vendor Specific Unique Unit Code Byte 4 Word

Table 20 — RW47: Vendor Specific Unique Unit Code Byte 4 Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	Byte 4 of Unique Unit Code[1] (Read Only)	Code 0
0	0	0	0	0	0	0	1		Code 1
0	0	0	0	0	0	1	0		Code 2
...									...
1	1	1	1	1	1	0	1		Code 253
1	1	1	1	1	1	1	0		Code 254
1	1	1	1	1	1	1	1		Code 255
NOTE 1 Programmed and locked in one time programmable memory by DDR5CKD01 vendor.									

5.4.9 RW48 - Vendor Specific Unique Unit Code Byte 5 Word

Table 21 — RW48: Vendor Specific Unique Unit Code Byte 5 Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	Byte 5 of Unique Unit Code[1] (Read Only)	Code 0
0	0	0	0	0	0	0	1		Code 1
0	0	0	0	0	0	1	0		Code 2
...									...
1	1	1	1	1	1	0	1		Code 253
1	1	1	1	1	1	1	0		Code 254
1	1	1	1	1	1	1	1		Code 255
NOTE 1 Programmed and locked in one time programmable memory by DDR5CKD01 vendor.									

5.4.10 RW49 - Vendor Specific Unique Unit Code Byte 6 Word

Table 22 — RW49: Vendor Specific Unique Unit Code Byte 6 Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	Byte 6 of Unique Unit Code[1] (Read Only)	Code 0
0	0	0	0	0	0	0	1		Code 1
0	0	0	0	0	0	1	0		Code 2
...									...
1	1	1	1	1	1	0	1		Code 253
1	1	1	1	1	1	1	0		Code 254
1	1	1	1	1	1	1	1		Code 255
NOTE 1 Programmed and locked in one time programmable memory by DDR5CKD01 vendor.									

5.4.11 RW4A - Vendor ID Byte 0 Word

Table 23 — RW4A: Vendor ID Byte 0 Word[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	Byte 0 of Vendor ID (Read Only)	VID[7:0] = 0x00h
0	0	0	0	0	0	0	1		VID[7:0] = 0x01h
0	0	0	0	0	0	1	0		VID[7:0] = 0x02h
...									...
1	1	1	1	1	1	0	1		VID[7:0] = 0xFDh
1	1	1	1	1	1	1	0		VID[7:0] = 0xFEh
1	1	1	1	1	1	1	1		VID[7:0] = 0xFFh
NOTE 1 Each vendor will have a specific Vendor ID value assigned by JEDEC.									

5.4.12 RW4B - Vendor ID Byte 1 Word

Table 24 — RW4B: Vendor ID Byte 1 Word[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	Byte 1 of Vendor ID (Read Only)	VID[15:8] = 0x00h
0	0	0	0	0	0	0	1		VID[15:8] = 0x01h
0	0	0	0	0	0	1	0		VID[15:8] = 0x02h
...									...
1	1	1	1	1	1	0	1		VID[15:8] = 0xFDh
1	1	1	1	1	1	1	0		VID[15:8] = 0xFEh
1	1	1	1	1	1	1	1		VID[15:8] = 0xFFh
NOTE 1 Each vendor will have a specific Vendor ID value assigned by JEDEC.									

5.4.13 RW4C - Device ID Byte 0 Word

Table 25 — RW4C: Device ID Byte 0 Word[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	Byte 0 of Device ID (Read Only)	DID[7:0] = 0x00h
0	0	0	0	0	0	0	1		DID[7:0] = 0x01h
0	0	0	0	0	0	1	0		DID[7:0] = 0x02h
...									...
1	1	1	1	1	1	0	1		DID[7:0] = 0xFDh
1	1	1	1	1	1	1	0		DID[7:0] = 0xFEh
1	1	1	1	1	1	1	1		DID[7:0] = 0xFFh
NOTE 1 The device ID value is 0x0531.									

5.4.14 RW4D - Device ID Byte 1 Word

Table 26 — RW4D: Device ID Byte 1 Word[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	Byte 1 of Device ID (Read Only)	DID[15:8] = 0x00h
0	0	0	0	0	0	0	1		DID[15:8] = 0x01h
0	0	0	0	0	0	1	0		DID[15:8] = 0x02h
...									...
1	1	1	1	1	1	0	1		DID[15:8] = 0xFDh
1	1	1	1	1	1	1	0		DID[15:8] = 0xFEh
1	1	1	1	1	1	1	1		DID[15:8] = 0xFFh
NOTE 1 The device ID value is 0x0531.									

5.4.15 RW4E - Vendor Revision ID Word

Table 27 — RW4E: Vendor Revision ID Word[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	Vendor Revision ID (Read Only)	RID[7:0] = 0x00h
0	0	0	0	0	0	0	1		RID[7:0] = 0x01h
0	0	0	0	0	0	1	0		RID[7:0] = 0x02h
...									...
1	1	1	1	1	1	0	1		RID[7:0] = 0xFDh
1	1	1	1	1	1	1	0		RID[7:0] = 0xFEh
1	1	1	1	1	1	1	1		RID[7:0] = 0xFFh
NOTE 1 Programmed and locked in one time programmable memory by DDR5CKD01 vendor.									

6 Absolute Maximum Ratings

Table 28 — Absolute Maximum Ratings over Operating Free-air Temperature Range[1]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	Supply voltage		–0.3	1.4	V
V_{IN}	Receiver input voltage[2]	See Note 4 and 5	–0.3	V_{DD} + 0.5	V
V_{OUT}	Driver output voltage[3]	See Note 4 and 5	–0.3	V_{DD} + 0.5	V
I_{IK}	Input clamp current	$V_{IN} < 0$ or $V_{IN} > V_{DD}$	-	-50	mA
I_{OK}	Output clamp current	$V_{OUT} < 0$ or $V_{OUT} > V_{DD}$	-	±50	mA
I_{OUT}	Continuous output current	$0 < V_{OUT} < V_{DD}$	-	±50	mA
I_{CCC}	Continuous current through each V_{DD} or V_{ss} pin		-	±100	mA
T_{stg}	Storage temperature		–55	+150	°C

NOTE 1 Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 2 This parameter does not apply to SCL. See Management Bus Interface chapter for voltage specifications for these inputs.

NOTE 3 This parameter does not apply to SDA. See Management Bus Interface chapter for voltage specifications for these inputs.

NOTE 4 The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

NOTE 5 This value is limited to 1.4 V maximum.

6.1 DC Operating and Temperature Conditions

The DDR5CKD01 parametric values are specified for the device default control word settings, unless otherwise stated.

Table 29 — DC Operating and Temperature Conditions

Symbol	Parameter	Condition	Min	Nom	Max	Unit
V_{DD}	DC Supply voltage[1]	1.1 V Operation	1.067 (-3%)	1.1	1.166 (+6%)	V
T_j	Junction temperature[2]		0	-	125	°C
T_{case}	Case temperature	Measurement procedure JESD51-2	-	-	103[3]	°C

NOTE 1 DC bandwidth limited to 20 MHz.

NOTE 2 For operation beyond Tj min and max datasheet values are not guaranteed and may de-rate. For operation above Tj max lifetime could be affected. All parametric measurements are performed at 0 °C, 25 °C, and 95 °C.

NOTE 3 This spec is meant to guarantee a Tj of 125 °C by the DDR5CKD01. Since Tj cannot be measured or observed by users, Tcase is specified instead. Under all thermal conditions, the Tj of a DDR5CKD01 shall not be higher than 125 °C

7 Input Electrical Characteristics and Timing

7.1 Input Clock Architecture

The CKD is provided a clock by the entity that is controlling it, i.e., memory controller, or any test equipment. This clock is used by the CKD to generate all the IO specific timing, and is the same clock used by the controlling entity as the one and only deterministic source of all the response timings to and from the CKD. This allows the memory controller to have a deterministic control of every event in the CKD. Spread Spectrum Clocking (SSC) Capability.

Note: Both PLL Bypass and Dual PLL modes require two input clock pairs.

7.2 Input Voltage and Timing Requirements

Table 30 — Input Voltage and Timing Requirements

Symbol	Parameter	Conditions	1000 to 4400 MHz		Unit
			Min	Max	
f_{CLOCK}	Input clock frequency[1]	Application frequency[2]	990	4466	MHz
V_{CM}	Average Common Mode DC Voltage where Vcm = (DCK_t voltage + DCK_c_voltage) / 2		0.22 x VDD	0.42 x VDD	mV
t_{CKDOP}	Minimum time from DRST_n transition HIGH to when CKD is operational.	t	10	-	µs
t_{DLOW}	Minimum clock stop power down time		10	-	ns
$V_{ILStatic}$	Low-Level input voltage when the device is in power savings mode	DCK_t / DCK_c single ended during clock stop event	-	0.12 x VDD[3]	mV
$V_{ILStatic_DC}$	Average Low-Level input voltage of DCK_t and DCK_c to put device into power savings mode	DCK_t / DCK_c single ended during clock stop event		0.05 x VDD	mV
t_{INIT0}	Maximum voltage-ramp time		-	20	ms
t_{INIT1}	Minimum DRST_n LOW time after completion of voltage ramp		200	-	µs
t_{PW_RESET}	Minimum DRST_n low time for Reset Initialization with stable power		1	-	µs
t_{INCK_OFFSET}	Maximum phase offset between the two input differential clock pairs DCK_A and DCK_B	Dual PLL Mode	- 0.5	0.5	t_{CK}

NOTE 1 Including SSC according Table 31, "SSC and PLL Loop Filter Characteristics,".
NOTE 2 All specified timing parameters apply
NOTE 3 Includes all sources of noise.

7.2 Input Voltage and Timing Requirements (cont'd)

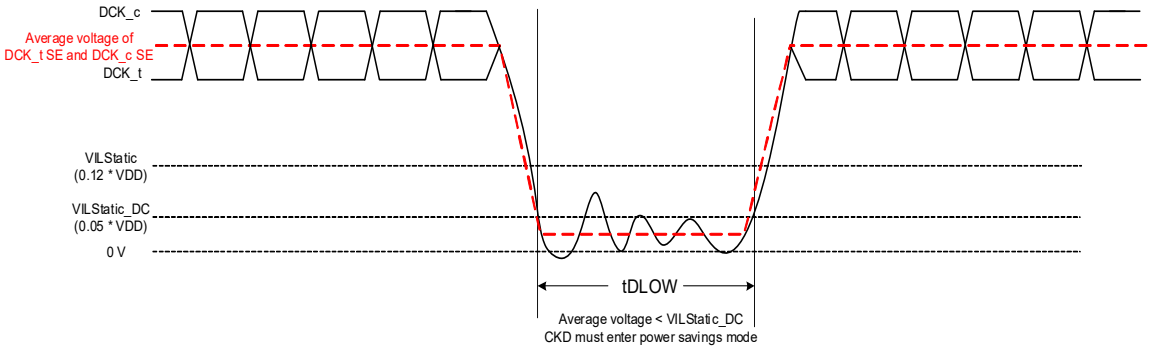


Figure 15 — $V_{ilStatic}$ DC Region

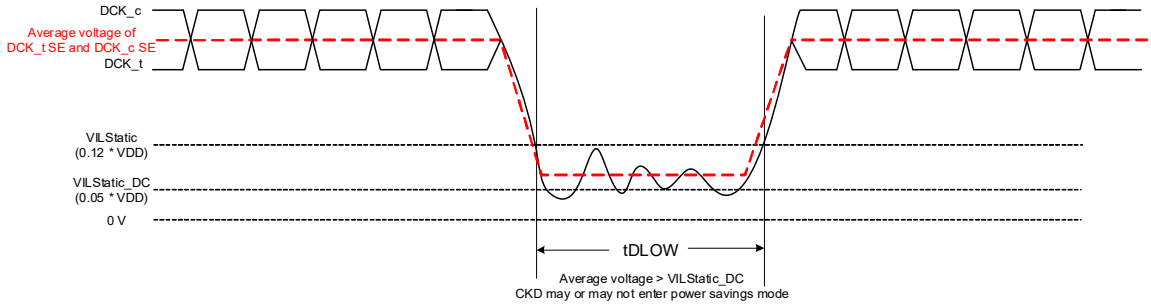


Figure 16 — $V_{ilStatic}$ Static Region

7.3 Input Clock SSC and PLL Loop Filter

The system platform uses a reference clock, which is used to synthesize the CKD clock. Spread Spectrum Clock (SSC) with up to 0.5% down-spread in frequency must be supported by the clocking system. The frequency of the reference clock, and therefore bit rate, can be modulated from 0% to –0.5% of the nominal data rate/frequency at a modulation rate in the range of 30 KHz to 33 KHz. The modulation profile of SSC must provide optimal or close to optimal EMI reduction. Typical profiles include a triangular profile. The CKD must ensure that it functions normally even in the presence of SSC and truthfully lets SSC related components pass through to its output signals.

Table 31 — SSC and PLL Loop Filter Characteristics

Symbol	Parameter	Conditions	1000 to 4400 MHz		Unit
			Min	Max	
f_{SSC}	SSC modulation frequency[1]		30	33	KHz
a_{SSC}	SSC amplitude[1]		0	-0.5	%
f_{band}	PLL loop bandwidth[2]	-3dB bandwidth[3]	0.02 x f_{clock}	-	MHz
NOTE 1	The DDR5CKD01 must meet all parameters defined in this specification while supporting input clock SSC requirements described in this table				
NOTE 2	The DDR5CKD01 PLL must fulfill this loop filter requirement in order to track typical system clock synthesizer output clock signals				
NOTE 3	Implies a jitter peaking of <3 dB				

7.4 Input Slew Rate for Differential Clock

Input slew rate for differential signals DCK_t/DCK_c are defined and measured as shown in Table 32.

Table 32 — Differential Input Slew Rate Definition for DCK_t/DCK_c

Symbol	Parameter	Measured		Units	Notes
		Min	Max		
V_{IHdiff_CK}	Differential Input High	0.75 * V_{DIFFpp}	-	mV	1, 2, 3, 4
V_{ILdiff_CK}	Differential input Low	-	0.25 * V_{DIFFpp}	mV	1, 2, 3, 4
NOTE 1 Clock V_{DIFFpp}, V_{ILdiff_CK} and V_{IHdiff_CK} are defined in Figure 17.					
NOTE 2 V_{DIFFpp} is the mean high voltage minus the mean low voltage over 1e6 samples.					
NOTE 3 Differential signal rising edge from V_{ILdiff_CK} to V_{IHdiff_CK} must be monotonic slope.					
NOTE 4 Differential signal falling edge from V_{IHdiff_CK} to V_{ILdiff_CK} must be monotonic slope.					

Table 33 — Differential Input Slew Rate DCK_t/DCK_c

Symbol	Parameter	Measured		Units	Notes
		Min	Max		
SRIdiff	Differential Input Slew Rate	2	15	V/ns	1
NOTE 1 All parameters are defined over the entire clock common mode range.					

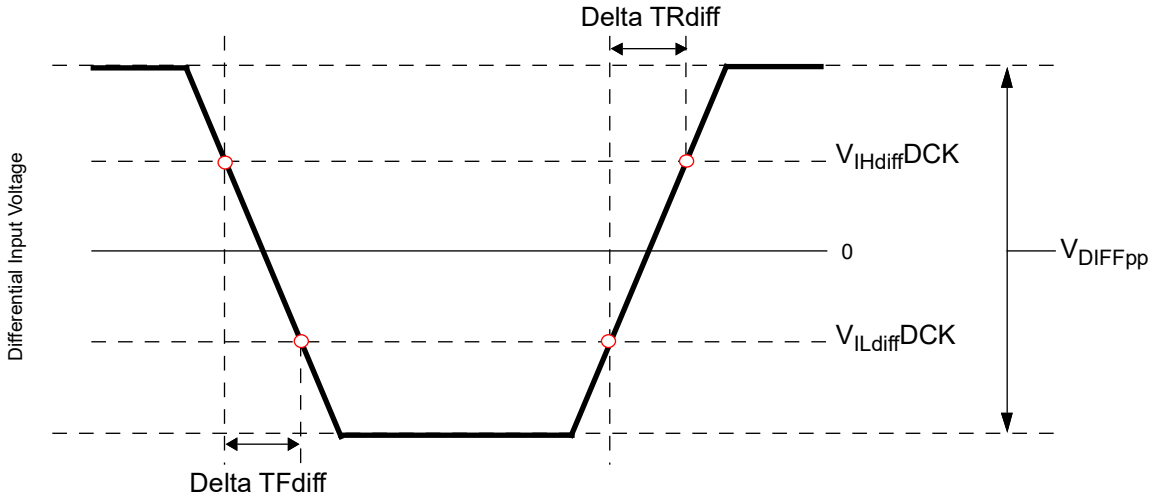


Figure 17 — Differential Input Slew Rate Definition for DCK_t/DCK_c

7.5 Differential Input Clock Cross Point Voltage

The differential input cross point voltage VIX_DCK (VIX_DCK_FR and VIX_DCK_RF) is measured from the actual cross point of DCK_t, DCK_c relative to the Vswing/2 of the DCK_t and DCK_c signals.

7.5 Differential Input Clock Cross Point Voltage (cont'd)

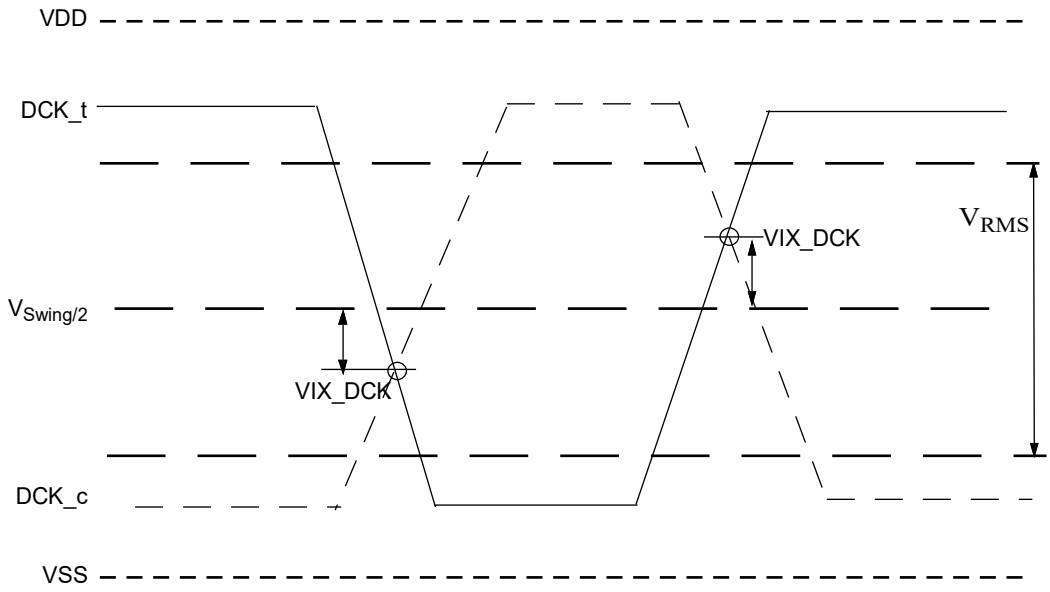


Figure 18 — Vix Definition (DCK)

Table 34 — Cross Point Voltage (VIX) for Differential Input Signals (DCK)

Symbol	Parameter	1000 to 3600 MHz		3800 to 4400 MHz		Unit	NOTE
		Min	Max	Min	Max		
VIX_CK_Ratio	Clock differential input crosspoint voltage ratio	-	50	-	TBD	%	1,2,3
NOTE 1	The VIX_CK voltage is referenced to V_{DCKMid}(mean) = (DCK_t voltage + DCK_c voltage) / 2, where the mean is over 100 tCK.						
NOTE 2	VIX_CK_Ratio = (|VIX_CK| / |V_{RMS}|) * 100%, where V_{RMS}= RMS(DCK_t voltage – DCK_c voltage).						
NOTE 3	Only applies when both DCK_t and DCK_c are transitioning and after tStab.						

7.6 Input Clock Termination (ICT) Characteristics for DCK

A functional representation of the input bus termination is shown in Figure 19. RTT= (V_{IN} / $|I_{IN}|$)

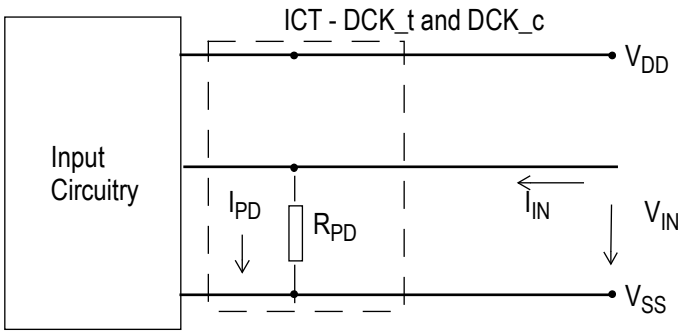


Figure 19 — Input Clock Termination: Definition of Voltages and Currents

7.6 Input Clock Termination (ICT) Characteristics for DCK (cont'd)

The DDR5CKD01 device supports an effective Input Clock Termination Rtt values. ICT Electrical Characteristics for DCK_t and DCK_c

Table 35 — ICT Electrical Characteristics for DCK_t and DCK_c

RTT	Vin	Min	Nom	Max	Unit	NOTE
120 Ω	VILdc= 0.05 * VDD	0.8	1	1.1	RZQ/2	1,2
	VIMdc= 0.35* VDD	0.9	1	1.1	RZQ/2	1,2
	VIHdc= 0.50 * VDD	0.9	1	1.25	RZQ/2	1,2
80 Ω	VILdc= 0.05 * VDD	0.8	1	1.1	RZQ/3	1,2
	VIMdc= 0.35 * VDD	0.9	1	1.1	RZQ/3	1,2
	VIHdc= 0.45 * VDD	0.9	1	1.25	RZQ/3	1,2
60 Ω	VILdc= 0.05 * VDD	0.8	1	1.1	RZQ/4	1,2
	VIMdc= 0.30 * VDD	0.9	1	1.1	RZQ/4	1,2
	VIHdc= 0.40 * VDD	0.9	1	1.25	RZQ/4	1,2
DCK_t - DCK_c Mismatch	VIMdc = 0.35 * VDD	0	-	8.0	%	

NOTE 1 For the behavior of the tolerance limits if temperature or voltage changes, see Section 8.5.1, "Output Driver and Termination Resistor Temperature and Supply Voltage Sensitivity,". If temperature and/or voltage change after calibration, the tolerance limits widen according to the tables shown below.

NOTE 2 Applies to DCK_t and DCK_c.

7.7 Input CMOS Rail-to-Rail Levels for DRST_n

Table 36 — CMOS Rail-to-Rail Input Levels for DRST_n

Symbol	Parameter	Min	Max	Unit	NOTE
VIH(AC)_RESET	AC Input High Voltage	0.8 * V_{DD}	V_{DD}	V	5
VIH(DC)_RESET	DC Input HIGH Voltage	0.7 * V_{DD}	VDD	V	2
VIL(DC)_RESET	DC Input LOW Voltage	VSS	0.3*VDD	V	1
VIL(AC)_RESET	AC Input LOW Voltage	VSS	0.2*VDD	V	6
TR_RESET	Rise Time	-	1.0	µs	
t_{PW_RESET}	RESET pulse width	1.0	-	µs	4
V_{SLPR_p2p}	Peak to peak voltage of slope reversal which must be suppressed	-	100	mV	3
t_{SLPRPW}	Pulse width of slope reversal which must be suppressed	-	10	ns	3

NOTE 1 After DRST_n is registered LOW, DRST_n level shall be maintained below VIL(DC)_RESET during tPW_RESET, otherwise, CKD PLL may not be reset.

NOTE 2 Once DRST_n is registered HIGH, DRST_n level must be maintained above VIH(DC)_RESET, otherwise, CKD operation will not be guaranteed until it is reset asserting DRST_n signal LOW.

NOTE 3 Slope Reversal (ringback) must remain below V_{SLPR_p2p} with the pulse width below $t_{SLPRPW.}$

NOTE 4 This definition is applied only "Reset Procedure with Power Stable."

NOTE 5 Overshoot might occur. It should be limited by the Absolute Maximum DC Ratings.

NOTE 6 Undershoot might occur. It should be limited by Absolute Maximum DC Ratings.

7.7 Input CMOS Rail-to-Rail Levels for DRST_n (cont'd)

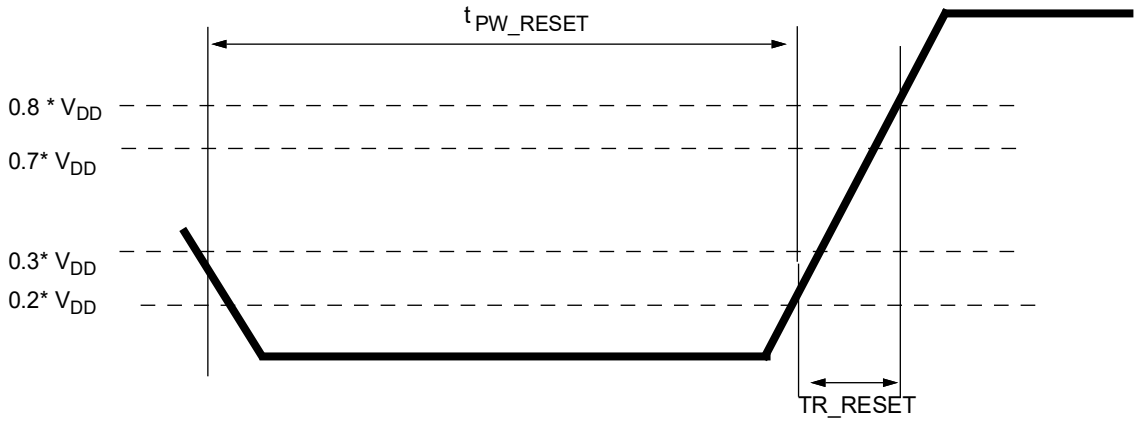


Figure 20 — tPW_RESET

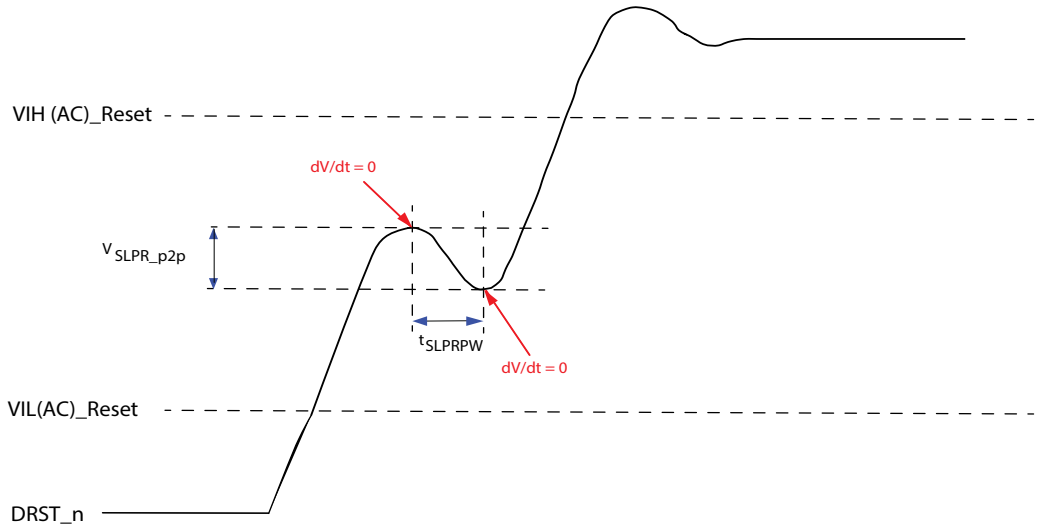


Figure 21 — DRST_n Slope Reversal

7.8 Differential Input Clock Voltage Sensitivity Parameter

Differential input clock (DCK_t, DCK_c) VRx_CK is defined and measured as shown below. The clock receiver must pass the minimum BER requirements for DDR5.

Table 37 — Rx Input Voltage Sensitivity Parameters for 1000 to 4400 MHz

Symbol	Parameter	1000 to 3200 MHz		3600 MHz		3800 to 4400 MHz		Unit
		MIn	Max	Min	Max	MIn	Max	
VRx_CK	Differential DCK_t/DCK_c Rx input voltage sensitivity (differential p-p).	-	130	-	120	-	TBD	mV
NOTE 1 Refer to the minimum BER 1e-9 requirements for DDR5.								
NOTE 2 This test should be done in typical temperature and voltage conditions (i.e., VDD = 1.1 V, 25 °C).								

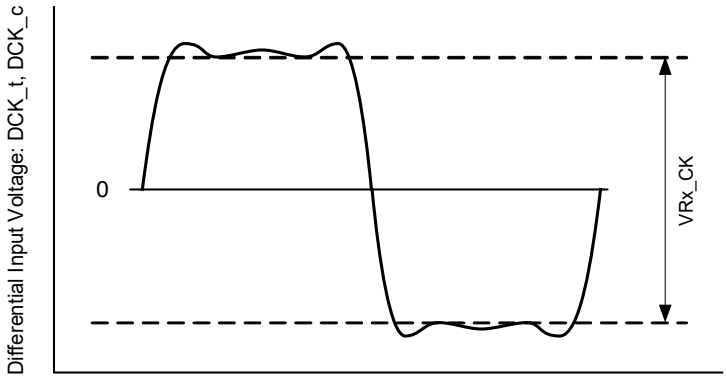


Figure 22 — VRx_CK

7.9 Input Clock Jitter

7.9.1 Overview

The clock is being driven to the CKD for modules, Figure 23.

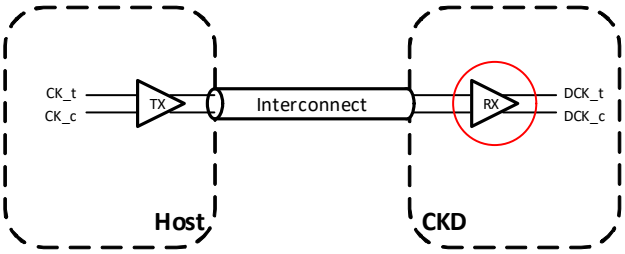


Figure 23 — Host Driving Clock Signals to the CKD

7.9.2 Specification for CKD Input Clock Jitter

The Random Jitter (Rj) specified is a random jitter meeting a Gaussian distribution. The Deterministic Jitter (Dj) specified is bounded. Input clock violating the min/max jitter values may result in malfunction of the DDR5CKD01 device.

Table 38 — Input Clock DCK Differential Jitter

[BUJ = Bounded Uncorrelated Jitter; DCD = Duty Cycle Distortion; Dj = Deterministic Jitter; Rj = Random Jitter; Tj = Total jitter; pp = Peak-to-Peak]

Symbol	Parameter	1000 to 3600 MHz		3800 to 4400 MHz		Unit	NOTE
		Min	Max	Min	Max		
tDCK	CKD Reference clock frequency	0.9999*f0	1.0001*f0	TBD	TBD	MHz	1
tDCK_Duty_Cycle	Duty Cycle	47.5	52.5	TBD	TBD	% tCK	4
tDCK_Duty_UI_Error	Duty Cycle Error	-	0.05	-	TBD	UI	1, 5
tDCK_1UI_Rj_NoBUJ	Rj value of 1-UI Jitter	-	0.006	-	TBD	UI (RMS)	3, 6
tDCK_1UI_Dj_NoBUJ	Dj pp value of 1-UI Jitter	-	0.030	-	TBD	UI	3,7
tDCK_1UI_Tj_NoBUJ	Tj value of 1-UI Jitter	-	0.13	-	TBD	UI	3,7
tDCK_NUI_Rj_NoBUJ	Rj value of N-UI Jitter	-	0.008	-	TBD	UI (RMS)	3,8
tDCK_NUI_Dj_NoBUJ	Dj pp value of N-UI Jitter	-	0.074	-	TBD	UI	3,9
tDCK_NUI_Tj_NoBUJ	Tj value of N-UI Jitter,	-	0.205	-	TBD	UI	3,9
tCK_NUI_Rj_NoBUJ, where N=4,5,6,...,30	Rj value of N-UI Jitter, where N=4,5,6,...,30		TBD		TBD	UI (RMS)	3, 11, 12, 13
tCK_NUI_Dj_NoBUJ, where N=4,5,6,...,30	Dj pp value of N-UI Jitter, N=4,5,6,...,30		TBD		TBD	UI	3, 11, 12, 13
tCK_NUI_Tj_NoBUJ, where N=4,5,6,...,30	Tj value of N-UI Jitter, N=4,5,6,...,30	-	TBD	-	TBD	UI	3, 11, 12, 13

Unit UI = tCK(avg).min/2

NOTE 1 f0 = Data Rate/2, example: if data rate is 3200MT/s, then f0=1600

NOTE 2 Rise and fall time slopes (V / nsec) are measured between +100 mV and -100 mV of the differential output of reference clock

NOTE 3 When there is no socket in transmitter measurement setup, in many cases, the contribution of the cross-talk is not significant or cannot be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining Tx lanes send patterns to the corresponding Rx receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specifications is met and another violated in which case the signaling analysis should be run to determine link feasibility

NOTE 4 Duty Cycle defined as the ratio between any even UI and tCK.

NOTE 5 Duty Cycle Error defined as absolute difference between average value of all UI with that of average of odd UI, which in magnitude would equal absolute difference between average of all UI and average of all even UI.

NOTE 6 Rj RMS value of 1-UI jitter without BUJ. This extraction is to be done after software correction of DCD

NOTE 7 Dj pp value of 1-UI jitter (after software assisted DCC). Without BUJ. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD

NOTE 8 Rj RMS value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 1 < N < 4. This extraction is to be done after software correction of DCD

NOTE 9 Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 1 < N < 4. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD

NOTE 10 Rj RMS value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 3 < N < 31. This extraction is to be done after software correction of DCD

NOTE 11 Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 3 < N < 31. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD

NOTE 12 The validation methodology for these parameters will be covered in future ballots

NOTE 13 If the clock meets total jitter Tj at BER of 1E-16, then meeting the individual Rj and Dj components of the spec can be considered optional. Tj is defined as Dj + 16.2*Rj for BER of 1E-16

8 Output Electrical Characteristics and Timings Output Clock Driver Characteristics

8.1 Output Clock Driver Characteristics

Table 39 — Output Clock Driver Characteristics at Application in PLL Modes

Symbol	Parameter	Conditions	1000 to 3600 MHz			3800 to 4400 MHz			Unit
			Min	Nom	Max	Min	Nom	Max	
t_{QOFF}	Time CKD to enter power savings mode and float QCK after DCK Stops	Clock Stop Power Down When the device is in Single or Dual PLL Mode	-	-	15	-	-	TBD	ns
t_{ODU}[1]	Output Delay Update time after CKD receives entire sideband command packet.to stable output clock	OP7 = 1 for RW04 to RW07	-	-	1	-	-	TBD	µs
t_{STAB}[2]	CKD Stabilization time from receiving Stable Input clock to PLL lock	DCK_t/DCK_c stable after the CKD becomes operational	-	-	1.0	-	-	TBD	µs
$t_{CKsk_PLL_Mode}$	Fractional Clock Output Skew per sub-channel[3]	When the device is in Single or Dual PLL mode	-	-	20	-	-	TBD	ps
$t_{staoff_PLL_MODE}$	Clock delay through the register between the input clock and output clock in PLL Mode	When device is in Single or Dual PLL Mode after t_{STAB}	- 50	0	70	- TBD	0	TBD	ps
$t_{dynoff_PLL_MODE}$	Maximum propagation delay variation over voltage and temperature within t_{staoff} window. This includes all sources of jitter and drift (e.g., thermal noise, supply noise, voltage/temperature drift, SSC tracking, etc.) except reference clock noise[4]	When device is in Single or Dual PLL Mode	-	-	30	-	-	TBD	ps

NOTE 1 This is the time CKD requires to update delay timing setting to the output after it receives RW write entire sideband command packet.

NOTE 2 t_{STAB} is PLL PHASE Lock not frequency lock t_{STAOFF} and jitter spec must be met after t_{STAB}.

NOTE 3 This skew represents the absolute output clock skew and contains the pad skew and package skew (See Figure 24). This parameter is specified for the clock pairs on each side of the CKD independently. The skew is applicable to either side clock pairs between QCK0_A_t/QCK0_A_c to QCK1_A_t/QCK1_A_c or QCK0_B_t/QCK0_B_c and QCK1_B_t/QCK1_B_c. This is not a tested parameter and has to be considered as a design goal only.

NOTE 4 See Figure 25, “Definition for tstaoff and tdynoff in Single and Dual PLL Mode”.

Table 40 — Output Clock Driver Characteristics at Application in PLL Bypass Mode

Symbol	Parameter	Conditions	1000 to 3000 MHz			Unit
			Min	Nom	Max	
$t_{CKsk_PLL_BYP}$	Fractional Clock Output Skew per sub-channel[1]	When device is in PLL_Bypass_Mode at 1000 to 3000 MHz	-	-	30	ps
$t_{staoff_PLL_BYP}$	Clock delay through the register between the input clock and output clock in PLL Bypass Mode	When device is in PLL Bypass Mode at 1000 to 3000 MHz	275	-	700	ps
$t_{dynoff_PLL_BYP}$	Maximum propagation delay variation over voltage and temperature within t_{staoff} window. This includes all sources of jitter and drift (e.g., thermal noise, supply noise, voltage/temperature drift, SSC tracking, etc.) except reference clock noise	When device is in PLL Bypass Mode at 1000 to 2800 MHz	-	-	60	ps

NOTE 1 This skew represents the absolute output clock skew and contains the pad skew and package skew (See Figure 24). This parameter is specified for the clock pairs on each side of the CKD independently. The skew is applicable to either side clock pairs between QCK0_A_t/QCK0_A_c to QCK1_A_t/QCK1_A_c or QCK0_B_t/QCK0_B_c and QCK1_B_t/QCK1_B_c. This is not a tested parameter and has to be considered as a design goal only.

8.1 Output Clock Driver Characteristics (cont'd)

Table 41 — Output Clock Driver Characteristics at Low Frequency PLL Bypass Test Mode

Symbol	Parameter	Conditions	Less than 990 MHz			Unit
			Min	Nom	Max	
$t_{Lowfreq_staoff_PLL_BYP}$	Clock delay through the register between the input clock and output clock in PLL Bypass Test Mode.[1]	When device is in PLL_Bypass_Mode less than 990 MHz	200	-	700	ps
$t_{Lowfreq_dynoff_PLL_BYP}$	Maximum propagation delay variation over voltage and temperature within $t_{Lowfreq_staoff_PLL_BYP}$ window. This includes all sources of skew, jitter and drift (e.g., thermal noise, supply noise, voltage/ temperature drift, SSC tracking, etc.) except reference clock noise [1]	When device is in PLL_Bypass_Mode less than 990 MHz in test environment	-	-	300	ps
NOTE 1 This Parameter is to support low speed module testing PLL Bypass Mode will run below 990 MHz. This parameter is not for normal PLL Bypass mode operating frequency range.						

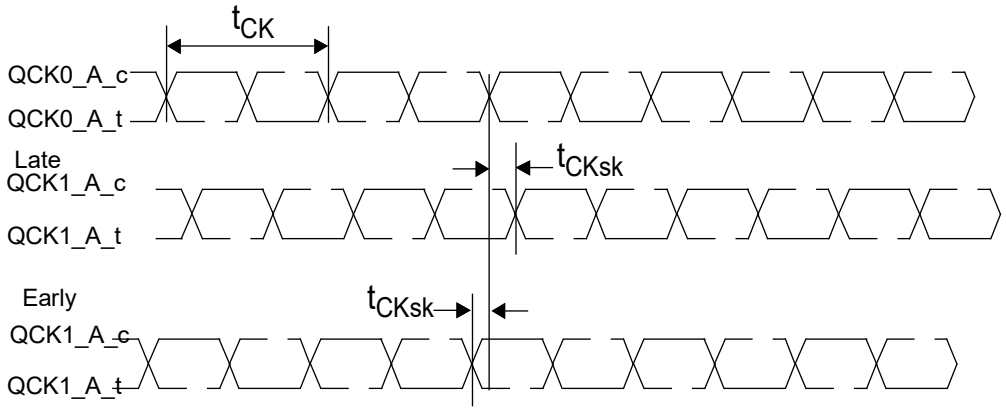


Figure 24 — Clock Output (QxCK) Skew

8.1 Output Clock Driver Characteristics (cont'd)

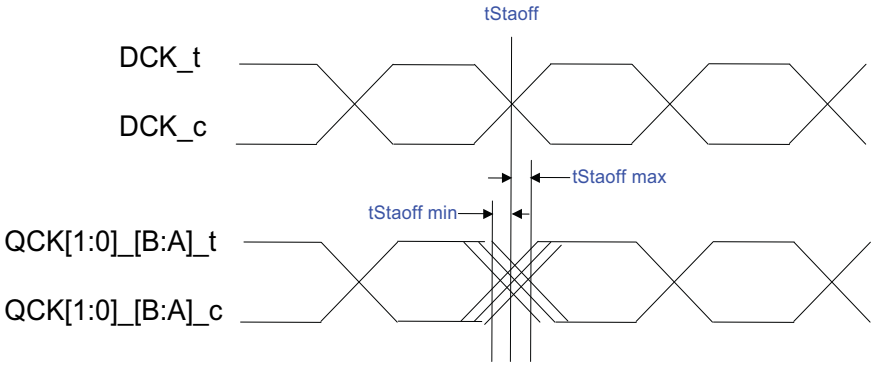
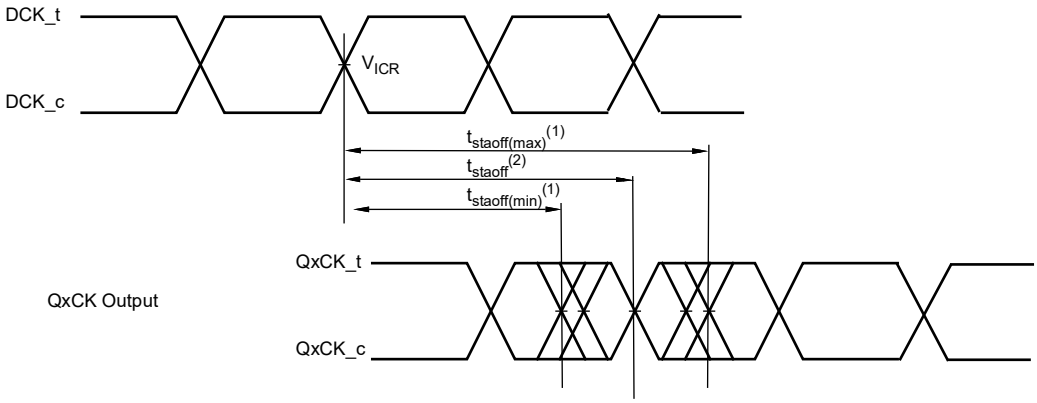


Figure 25 — Definition for tstaoff and tdynoff in Single and Dual PLL Mode

1. $t_{staoff(max/min)}$ = Propagation delay specification limits for clock signal for corresponding data cycles over proess, voltage, and temperature.
2. t_{staoff} = Measured propagation delay for clock signal for corresponding data cycles.
3. t_{dynoff} = maximum propagation delay variation over voltage and temperature within t_{staoff} window. This includes all sources of jitter and drift (e.g., thermal noise, supply noise, voltage/temperature drift, SSC tracking) except reference clock noise.



V_{ICR}: Cross Point Voltage

Figure 26 — Definition for tstaoff and tdynoff in PLL Bypass Mode

1. $t_{staoff(max/min)}$ = propagation delay specification limits for clock signal over process, voltage and temperature.
2. t_{staoff} = measured propagation delay for clock signal for corresponding data cycles.
3. t_{dynoff} = maximum propagation delay variation over voltage and temperature within t_{staoff} window. This includes all sources of jitter and drift (e.g., thermal noise, supply noise, voltage/temperature drift, SSC tracking, etc.) except reference clock noise.

8.2 Output Clock Differential Slew Rate Definition for QnCK_t / QnCK_c

Output slew rates for differential signals QnCKx_t / QnCKx_c are defined and measured as shown in Table 42 and Figure 27.

Table 42 — Output Clock Differential Slew Rate Definition for QnCK_t / QnCK_c

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge (QnCK_t / QnCK_c .	25%*Total swing	75% *Total swing	[|25% - 75%|] / DeltaTRdiff
Differential output slew rate for falling edge (QnCK_t / QnCK_c).	75%*Total swing	25% *Total swing	[|75% - 25%|] / DeltaTFdiff
NOTE Differential output slew rate is verified by design and characterization, and may not be subject to production test.			

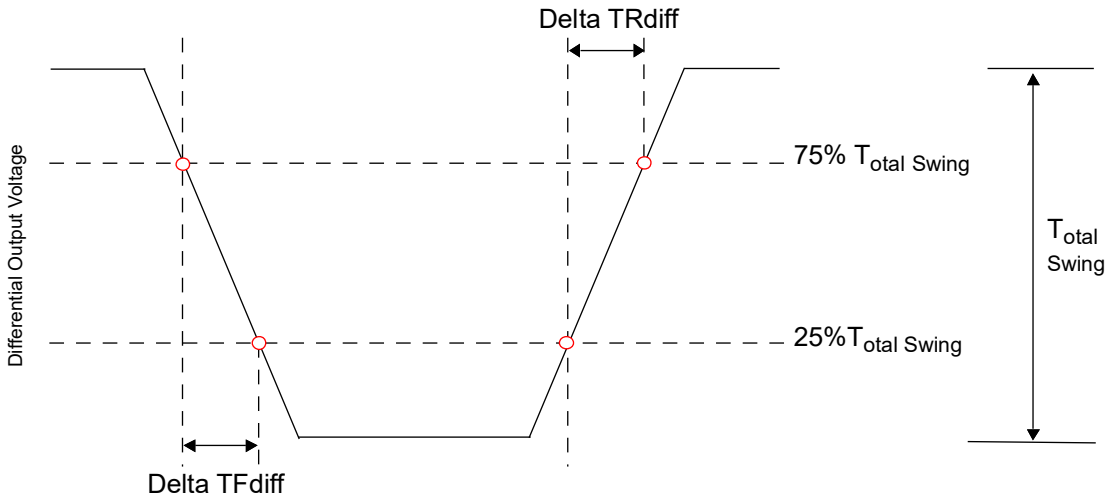


Figure 27 — Differential Output Slew Rate Definition for QnCK_t / QnCK_c

8.2.1 Output Differential Edge Rate

Table 43 — Output Differential Edge Rates[1]

Symbol	Parameter	Conditions	1000 to 4400 MHz		Unit
			Min	Max	
dV/dt_r	QCK rising edge differential Slew Rate	1.1 V operation	16	37	V/ns
dV/dt_f	QCK falling edge differential Slew Rate	1.1 V operation	16	37	V/ns
dV/dt_D[2]	Absolute difference between dV/dt_r and dV/dt_f	1.1 V operation	-	4	V/ns
NOTE 1 There are two selectable output slew rate ranges defined for QCK in RW03 respectively. See Table Table 9, "RW03 - QCK Output Differential Slew Rate Control Word,", for operating conditions.					
NOTE 2 Difference between dV/dt_r (rising edge rate) and dV/dt_f (falling edge rate)					

8.3 Output Differential Slew Rate Control

Table 44 — Output Differential Slew Rate Control

Symbol	Parameter	1000 to 4400 MHz		Unit
		Min	Max	
QnCK_t/QnCK_c Differential Slew Rate				
SR_{MOD}	Moderate	16	30	V/ns
SR_{Fast}	Fast	20	37	V/ns

8.4 Differential Output Clock Cross Point Voltage

The differential output clock cross point voltage is defined as the cross point voltage measured on the differential signals QnCK_t / QnCK_c with respect to the output common mode voltage (V_{OCM}).

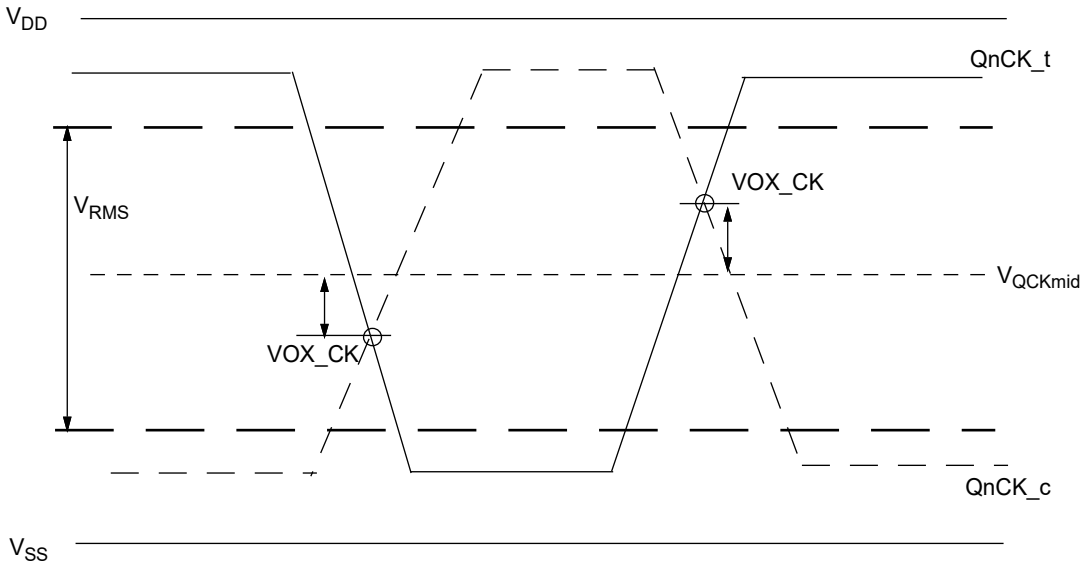


Figure 28 — VOX Definition for QnCK_t/QnCK_c

Table 45 — Output Cross Point Voltage for QnCK_t/QnCK_c

Symbol	Parameter	1000 to 3600 MHz		3800 to 4400 MHz		Unit	NOTE
		Min	Max	Min	Max		
VOX_CK_Ratio	QnCK Differential Output Cross-Point Voltage Ratio	-	20	-	TBD	%	1,2,3

NOTE 1 Referenced to VQCKmid= avg (QnCK_t + QnCK_c)/2, where the average is over 100 tCK.
NOTE 2 VOX_CK_Ratio = (|VOX_CK| / |V_{RMS}|)*100%, where V_{RMS} = RMS(QnCK_t voltage - QnCK_c).
NOTE 3 Only applies when both QnCK_t and QnCK_c are transitioning. Measured into 50-Ω reference load terminated to V_{DD}, as shown in Figure 31
NOTE 4 Measured at output slew rate setting Moderate.and driver strength Moderate .

8.5 Output R-on Drive Specifications per Drive Strength Setting

Table 46 — Output Ron Drive

Symbol	Parameter	1000 to 4400 MHz			Unit
		Min	Nom	Max	
QnCK_t/QnCK_c					
R_{onWD}	Weak Drive (34 Ω)	see Table 47	$R_{ZQ}/7$	see Table 47	Ω
R_{onLD}	Light Drive (27 Ω)		$R_{ZQ}/9$		Ω
R_{onMD}	Moderate Drive (20 Ω)		$R_{ZQ}/12$		Ω
R_{onSD}	Strong Drive (14 Ω)		$R_{ZQ}/17$		Ω

NOTE 1 A functional representation of the output buffer is shown in Figure 29. Output impedance RON is defined by the value of the external reference resistor R_{ZQ} as defined in Table 47.

The individual pull-up and pull-down resistors (RON_{Pu} and RON_{Pd}) are defined as follows:

$$RON_{Pu} = \frac{V_{DD} - V_{Out}}{|I_{Out}|} \quad \text{under the condition that } RON_{Pd} \text{ is turned off.} \tag{1}$$

$$RON_{Pd} = \frac{V_{Out}}{|I_{Out}|} \quad \text{under the condition that } RON_{Pu} \text{ is turned off.}$$

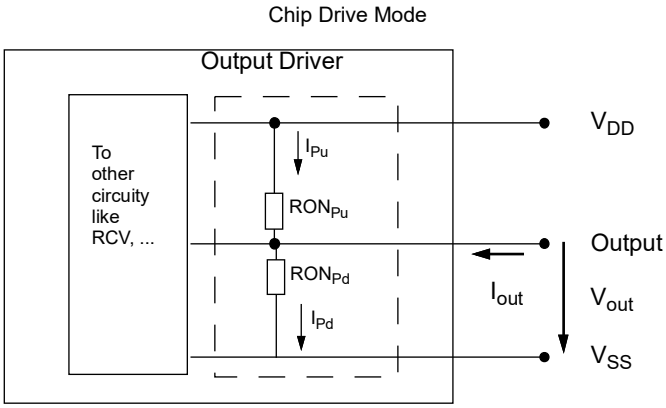


Figure 29 — Output Driver: Definition of Voltages and Currents

NOTE 2 Assuming R_{ZQ} = 240 Ω +/- 1%

8.5 Output R-on Drive Specifications per Drive Strength Setting (cont'd)

Table 47 — Output Driver DC Electrical Characteristics, Entire Operating Temperature Range

RON_{Nom}	Resistor	V_{Out}	Min	Nom	Max	Unit	NOTE
34 Ω Weak Drive	RON_{34Pd}	$V_{OLdc} = 0.5 \times V_{DD}$	0.8	1.0	1.1	$R_{ZQ}/7$	1, 2
		$V_{OMdc} = 0.8 \times V_{DD}$	0.9	1.0	1.1	$R_{ZQ}/7$	1, 2
		$V_{OHdc} = 0.95 \times V_{DD}$	0.9	1.0	1.25	$R_{ZQ}/7$	1, 2
	RON_{34Pu}	$V_{OLdc} = 0.5 \times V_{DD}$	0.9	1.0	1.25	$R_{ZQ}/7$	1, 2
		$V_{OMdc} = 0.8 \times V_{DD}$	0.9	1.0	1.1	$R_{ZQ}/7$	1, 2
		$V_{OHdc} = 0.95 \times V_{DD}$	0.8	1.0	1.1	$R_{ZQ}/7$	1, 2
27 Ω Light Drive	RON_{27Pd}	$V_{OLdc} = 0.5 \times V_{DD}$	0.8	1.0	1.1	$R_{ZQ}/9$	1, 2
		$V_{OMdc} = 0.8 \times V_{DD}$	0.9	1.0	1.1	$R_{ZQ}/9$	1, 2
		$V_{OHdc} = 0.95 \times V_{DD}$	0.9	1.0	1.25	$R_{ZQ}/9$	1, 2
	RON_{27Pu}	$V_{OLdc} = 0.5 \times V_{DD}$	0.9	1.0	1.25	$R_{ZQ}/9$	1, 2
		$V_{OMdc} = 0.8 \times V_{DD}$	0.9	1.0	1.1	$R_{ZQ}/9$	1, 2
		$V_{OHdc} = 0.95 \times V_{DD}$	0.8	1.0	1.1	$R_{ZQ}/9$	1, 2
20 Ω Moderate Drive	RON_{20Pd}	$V_{OLdc} = 0.5 \times V_{DD}$	0.8	1.0	1.1	$R_{ZQ}/12$	1, 2
		$V_{OMdc} = 0.8 \times V_{DD}$	0.9	1.0	1.1	$R_{ZQ}/12$	1, 2
		$V_{OHdc} = 0.95 \times V_{DD}$	0.9	1.0	1.25	$R_{ZQ}/12$	1, 2
	RON_{20Pu}	$V_{OLdc} = 0.5 \times V_{DD}$	0.9	1.0	1.25	$R_{ZQ}/12$	1, 2
		$V_{OMdc} = 0.8 \times V_{DD}$	0.9	1.0	1.1	$R_{ZQ}/12$	1, 2
		$V_{OHdc} = 0.95 \times V_{DD}$	0.8	1.0	1.1	$R_{ZQ}/12$	1, 2
14 Ω Strong Drive	RON_{14Pd}	$V_{OLdc} = 0.5 \times V_{DD}$	0.8	1.0	1.1	$R_{ZQ}/17$	1, 2
		$V_{OMdc} = 0.8 \times V_{DD}$	0.9	1.0	1.1	$R_{ZQ}/17$	1, 2
		$V_{OHdc} = 0.95 \times V_{DD}$	0.9	1.0	1.25	$R_{ZQ}/17$	1, 2
	RON_{14Pu}	$V_{OLdc} = 0.5 \times V_{DD}$	0.9	1.0	1.25	$R_{ZQ}/17$	1, 2
		$V_{OMdc} = 0.8 \times V_{DD}$	0.9	1.0	1.1	$R_{ZQ}/17$	1, 2
		$V_{OHdc} = 0.95 \times V_{DD}$	0.8	1.0	1.1	$R_{ZQ}/17$	1, 2
Mismatch between pull-up and pull-down, $_{MMPuPd}$		$V_{OHdc} = 0.8 \times V_{DD}$	-10	-	10	%	1,2,3
Mismatch within component variation pull-up $_{MMPudd}$		$V_{OHdc} = 0.8 \times V_{DD}$	0	-	10	%	1,2,4
Mismatch within component variation pull-down $_{MMPddd}$		$V_{OHdc} = 0.8 \times V_{DD}$	0	-	10	%	1,2,4

NOTE 1 The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see Section 8.5.1, "Output Driver and Termination Resistor Temperature and Supply Voltage Sensitivity,".

NOTE 2 Pull-up and pull-down output driver impedances are recommended to be calibrated at $0.8 * V_{DD}$. Other calibration schemes may be used to achieve the linearity spec shown above, e.g., calibration at $0.5 * V_{DD}$ and $0.95 * V_{DD}$.RON variance range ratio to RON nominal value in a given component.

NOTE 3 Measurement definition for mismatch between pull-up and pull-down, MM_{PuPd}: Measure RON_{Pu} and RON_{Pd}, both at 0.8 * VDD (for the other impedances) separately. Ron-nom is the nominal Ron value:

$$MM_{PuPd} = \frac{RON_{Pu} - RON_{Pd}}{RON_{Nom}} x100$$

NOTE 4 RON variance range ratio to RON nominal value in a given component.

$$MM_{Pudd} = \frac{RON_{PuMax} - RON_{PuMin}}{RON_{Nom}} x100$$

$$MM_{Pddd} = \frac{RON_{PdMax} - RON_{PdMin}}{RON_{Nom}} x100$$

8.5.1 Output Driver and Termination Resistor Temperature and Supply Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to Table 48 and Table 49.

Table 48 — Output Driver and Termination Resistor Sensitivity Definition

Resistor	Definition Point	Min	Max	Unit	NOTE
R_{ONPD}	0.8 x VDD	90 - ($dR_{ONPD}dT$ x |ΔT|) - ($dR_{ONPD}dV$ x |ΔV|)	110+($dR_{ONPD}dT$ x |ΔT|) + ($dR_{ONPD}dV$ x |ΔV|)	%	1,2
R_{ONPU}	0.8 x VDD	90 - (dR_{ONPU} x |ΔT|) - (dR_{ONPU} x |ΔV|)	110 +(dR_{ONPU} x |ΔT|) + (dR_{ONPU} x |ΔV|)	%	1,2
R_{ICT}	0.3 x VDD	90 - ($dR_{ICT}dT$ x |ΔT|) - ($dR_{ICT}dV$ x |ΔV|)	110 + ($dR_{ICT}dT$ x |ΔT|) + ($dR_{ICT}dV$ x |ΔV|)	%	1,2,3

NOTE 1 ΔT = T - T(@ Calibration), ΔV = V - V(@ Calibration)
NOTE 2 $dR_{ONPD}dT$, $dR_{ONPD}dV$, $dR_{ONPU}dT$, $dR_{ONPU}dV$, $dR_{ICT}dV$, and $dR_{ICT}dT$ are not subject to production test but are verified by design and characterization.
NOTE 3 This parameter applies to Input pins DCK_[B:A]_t/DCK[B:A]_c

Table 49 — Output Driver and Termination Resistor Temperature and Voltage Sensitivity

Symbol	Parameter	Min	Max	Unit
$dR_{ONPD}dT$	R_{ONPD} Temperature Sensitivity	0.00	0.1	%/°C
$dR_{ONPD}dV$	R_{ONPD} Voltage Sensitivity	0.00	0.1	%/mV
$dR_{ONPU}dT$	R_{ONPU} Temperature Sensitivity	0.00	0.1	%/°C
$dR_{ONPU}dV$	R_{ONPU} Voltage Sensitivity	0.00	0.1	%/mV
$dR_{ICT}T$	R_{ICT} Temperature Sensitivity	0.00	0.1	%/°C
$dR_{ICT}dV$	R_{ICT} Voltage Sensitivity	0.00	0.1	%/mV

8.6 Differential Output Clock Driver Jitter Characteristics

8.6.1 Overview

The Random Jitter (Rj) specified is a random jitter meeting Gaussian distribution. The Deterministic Jitter (Dj) specified is bounded. The DDR5 device output jitter must not exceed maximum values specified in Table 38.

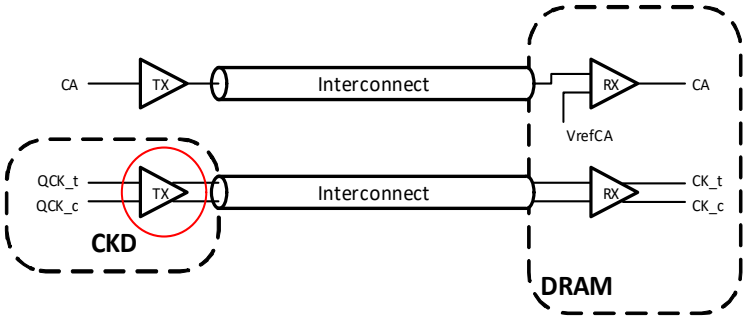


Figure 30 — Example of QCK TX Interconnect

8.6.2 Tx QCK Jitter Specifications for Single and Dual PLL Modes

Table 50 — Tx QCK Jitter Specifications for Single and Dual PLL Modes 1000 to 4400 MHz

[BUJ = Bounded Uncorrelated Jitter; DCD = Duty Cycle Distortion; Dj = Deterministic Jitter; Rj = Random Jitter; pp = Peak-to-Peak]

Symbol	Parameter	1000 to 3200 MHz		3600 MHz		3800 to 4400 MHz		Unit	NOTE
		Min	Max	Min	Max	Min	Max		
tTx_QCK_Duty_Cycle	Duty Cycle	47.5	52.5	47.5	52.5	TBD	TBD	% tCK	4, 12
tTx_QCK_1UI_Rj_NoBUJ	Rj value of 1-UI Jitter without BUJ	-	0.003	-	0.003	-	TBD	UI (RMS)	1, 2, 3
tTx_QCK_1UI_Dj_NoBUJ	Dj pp value of 1-UI Jitter without BUJ	-	0.025	-	0.025	-	TBD	UI	1, 3, 4
tTx_QCK_NUI_Rj_NoBUJ	Rj value of N-UI Jitter without BUJ	-	0.003	-	0.003	-	TBD	UI (RMS)	1, 3, 5
tTx_QCK_NUI_Dj_NoBUJ	Dj pp value of N-UI Jitter without BUJ	-	0.07	-	0.06	-	TBD	UI	1, 3, 6
tCK_NUI_Rj_NoBUJ, where N=4,5,6,...,30	Rj value of N-UI Jitter, where N=4,5,6,...,30	-	TBD	-	TBD	-	TBD	UI (RMS)	1, 3,
tCK_NUI_Dj_NoBUJ, where N=4,5,6,...,30	Dj pp value of N-UI Jitter, N=4,5,6,...,30	-	TBD	-	TBD	-	TBD	UI	1, 3, 8

Unit UI = tCK(avg).min/2

NOTE 1 When there is no socket in transmitter measurement setup, in many cases, the contribution of the cross-talk is not significant or cannot be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining Tx lanes send patterns to the corresponding Rx receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specifications is met and another violated in which case the signaling analysis should be run to determine link feasibility.

NOTE 2 Rj RMS value of 1-UI jitter without BUJ. This extraction is to be done after software correction of DCD.

NOTE 3 This test should be done in typical temperature and voltage conditions (i.e., V_{DD} = 1.1 V, 25 °C)

NOTE 4 Dj pp value of 1-UI jitter (after software assisted DCC). Without BUJ. Dj indicates Djdd of dual-Dirac fitting.

NOTE 5 Rj RMS value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 1 < N < 4. This extraction is to be done after software correction of DCD.

NOTE 6 Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 1 < N < 4. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD.

NOTE 7 Rj RMS value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 3 < N < 31. This extraction is to be done after software correction of DCD.

NOTE 8 Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 3 < N < 31. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD.

8.6.3 Tx QCK Jitter Specifications for PLL Bypass Mode

Input Clock Jitter DCK + Induced Device Jitter Bypass = TX Jitter Bypass

Table 51 — Tx QCK Jitter Specifications for PLL Bypass Mode 1000 to 3000 MHz

[BUJ = Bounded Uncorrelated Jitter; DCD = Duty Cycle Distortion; Dj = Deterministic Jitter; Rj = Random Jitter; pp = Peak-to-Peak]

Symbol	Parameter	1000 to 3000 MHz		Unit	NOTE
		Min	Max		
tQCK Duty_Cycle_Bypass	Duty Cycle in Bypass Mode	Min(tDCK_Duty_Cycle) - TBD	Max(tDCK_Duty_Cycle) + TBD	%tCK	
tTx_QCK_1UI_Rj_NoBUJ_Bypass	Rj value of 1-UI Jitter without BUJ in Bypass Mode	-	Sqrt [(tDCK_1UI_Rj_NoBUJ)^2 + 0.003^2]	UI (RMS)	1, 2, 3
tTx_QCK_1UI_Dj_NoBUJ_Bypass	Dj pp value of 1-UI Jitter without BUJ	-	tDCK_1UI_Dj_NoBUJ + 0.01	UI	1, 3, 4
tTx_QCK_NUI_Rj_NoBUJ_Bypass	Rj value of N-UI Jitter without BUJ	-	Sqrt [(tDCK_NUI_Rj_NoBUJ)^2 + 0.003^2]	UI (RMS)	1, 3, 5
tTx_QCK_NUI_Dj_NoBUJ_Bypass	Dj pp value of N-UI Jitter without BUJ	-	tDCK_NUI_Dj_NoBUJ + 0.02	UI	1, 3, 6

Unit UI = tCK(avg).min/2

NOTE 1 When there is no socket in transmitter measurement setup, in many cases, the contribution of the cross-talk is not significant or cannot be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining Tx lanes send patterns to the corresponding Rx receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specifications is met and another violated in which case the signaling analysis should be run to determine link feasibility.

NOTE 2 Rj RMS value of 1-UI jitter without BUJ. This extraction is to be done after software correction of DCD.

NOTE 3 This test should be done in typical temperature and voltage conditions (i.e., V_{DD} = 1.1 V, 25 °C).

NOTE 4 Dj pp value of 1-UI jitter (after software assisted DCC). Without BUJ. Dj indicates Djdd of dual-Dirac fitting.

NOTE 5 Rj RMS value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 1 < N < 4. This extraction is to be done after software correction of DCD.

NOTE 6 Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 1 < N < 4. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD.

9 Input/Output Capacitance and ESD

9.1 Silicon Pad I/O Capacitance

Table 52 — Silicon Pad I/O Capacitance Values

Symbol	Parameter	1000 to 4400 MHz		Unit	NOTES
		Min	Max		
C_O	Output capacitance QCK_t,QCK_c	-	1.5	pF	1,2
C_{CK}	Input capacitance, DCK_t, DCK_c	0.2	0.95	pF	1
C_{DCK}	Input capacitance delta DCK_t and DCK_c	-	0.1	pF	1, 3
C_{IR}	Input capacitance, DRST_n	0.5	3.5	pF	1, 4

NOTE 1 This parameter does not include package capacitance.
NOTE 2 Applies to QxCKy_N_t, and QxCKy_N_c.
NOTE 3 Absolute value of DCK_t - DCK_c
NOTE 4 Parameter specified at VI = VDD or VSS; VDD = 1.1 V

9.1 Silicon Pad I/O Capacitance (cont'd)

Table 53 — Package Electrical Characteristics

Symbol	Parameter	1000 to 4400 MHz		Unit	Notes
		Min	Max		
ZI_{DCK_DIFF}	Input DCK pins Zpkg	60	90	Ω	1, 2, 11
TdI_{DCK}	Input DCK pins Pkg Delay	-	25	ps	1, 3
ZO_{QCK_DIFF}	Output QnCK pins Zpkg	45	80	Ω	1, 2, 11
TdO_{QCK}	Output QnCK pins Pkg Delay	-	25	ps	1, 3
$DTdO_{QCK}$	Delta Delay between all QxCKy_N for a sub-channel	-	5	ps	1, 5
DZI_{DCK}	Delta Zpkg DCK_t and DCK_c	-	1	Ω	1, 2, 7
$DTdI_{DCK}$	Delta Delay DCK_t and DCK_c	-	1	ps	1, 8
DZO_{QCK}	Delta Zpkg QxCK_t and QxCK_c	-	3	Ω	1, 2, 9
$DTdO_{QCK}$	Delta Delay QxCK_t and QxCKn_c	-	4	ps	1,10
ZI_{DRST}	Input DRST Zpkg	40	70	Ω	1, 2
TdI_{DRST}	Input DRST Pkg Delay	5	25	ps	1, 3
ZI_{SDA_SCL}	Input SDA/SCL Zpkg	40	70	Ω	1, 2
TdI_{SDA_SCL}	Input SDA/SCL Pkg Delay	5	25	ps	1, 3

NOTE 1 This parameter is not subject to production test. It is verified by design and characterization. The package parasitics are determined using package only samples.
NOTE 2 This parameter is measured by using vendor specific measurement methodology to calculate the average Zpkg_xx over the interval Tpkg_delay_xx
NOTE 3 This parameter is measured by using vendor specific measurement methodology
NOTE 4 Absolute value of MAX(ZI_{QCK})-MIN(ZI_{QCK}) per sub-channel.
NOTE 5 Absolute value of MAX(TdO_{QCK})-MIN(TdO_{QCK}) per sub-channel.
NOTE 6 Single-ended impedance.
NOTE 7 Absolute value of ZIDCK_t - ZIDCK_c.
NOTE 8 Absolute value of TdIDCK_t - TdIDCK_c.
NOTE 9 Absolute value of ZOQxCK_N_t - ZOQxCK_N_c.
NOTE 10 Absolute value of TdOQxCK_N_t - TdOQxCK_N_c.
NOTE 11 Differential impedance.

9.2 Electrostatic Discharge Sensitivity Characteristics

Table 54 — Electrostatic Discharge Sensitivity Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
Human body model (HBM)	ESD_{HBM}	1000	-	V	1, 2
Charged-device model (CDM)	ESD_{CDM}	250	-	V	1, 3

NOTE 1 State-of-the-art basic ESD control measures have to be in place when handling devices.
NOTE 2 Refer to JEDEC / ESDA Joint Standard JS-001 for measurement procedures.
NOTE 3 Refer to ANSI / ESDA / JEDEC Joint Standard JS-002 f for measurement procedures.

10 DDR5CKD01 Reference Load

10.1 Test Circuits and Switching Waveforms

The circuit in Figure 31 represents the effective reference load of 50 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

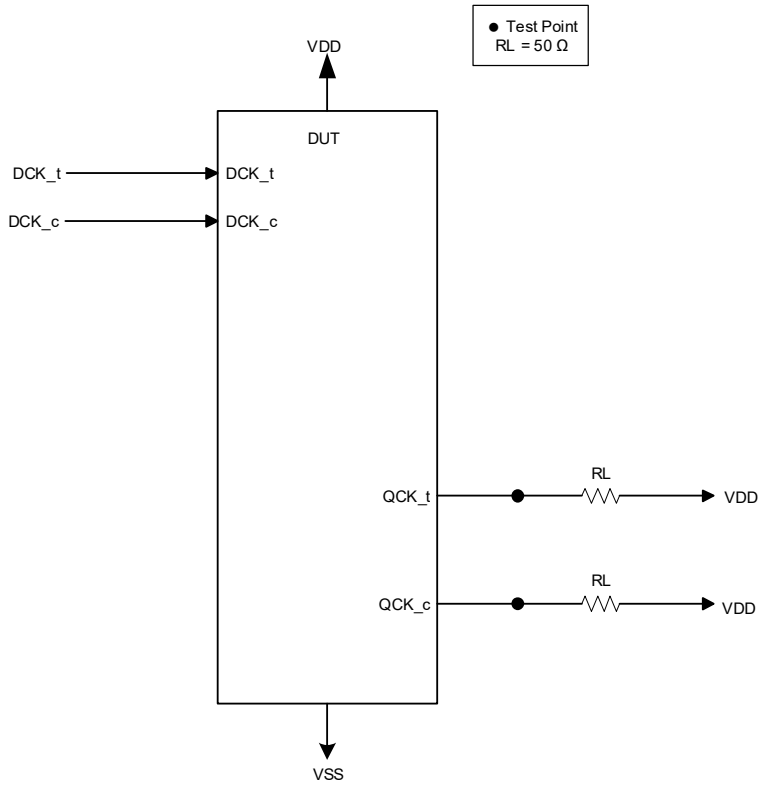


Figure 31 — Test Load

11 IDD Specification

In this chapter, IDD measurement conditions such as test load and patterns are defined. Figure 32 shows the setup and test load for IDD measurements.

- IDD currents (such as IDD4A, IDD4B, IDD6R and IDD6S) are measured as time-averaged currents with all V_{DD} balls of the DDR5CKD01 under test tied together.
- IDD currents can be measured for each speed bin. Each measurement shall use the minimum tCK (avg) for each speed bin.
- **ATTENTION:** IDD values cannot be directly used to calculate IO power of the DDR5CKD01. They can be used to support correlation of simulated IO power to actual IO power as outlined in Figure 33.

For IDD measurements, the following definitions apply:

- Basic IDD Measurement Conditions are described in Table 55.

IDD Measurements are done after properly initializing the DDR5CKD01. This includes but is not limited to setting

- All clock outputs enabled per channel in RW00;
- ICT 60 Ω
- All output driver strength set to RZQ/17;

ATTENTION: The IDD Measurements must run for TBD s.

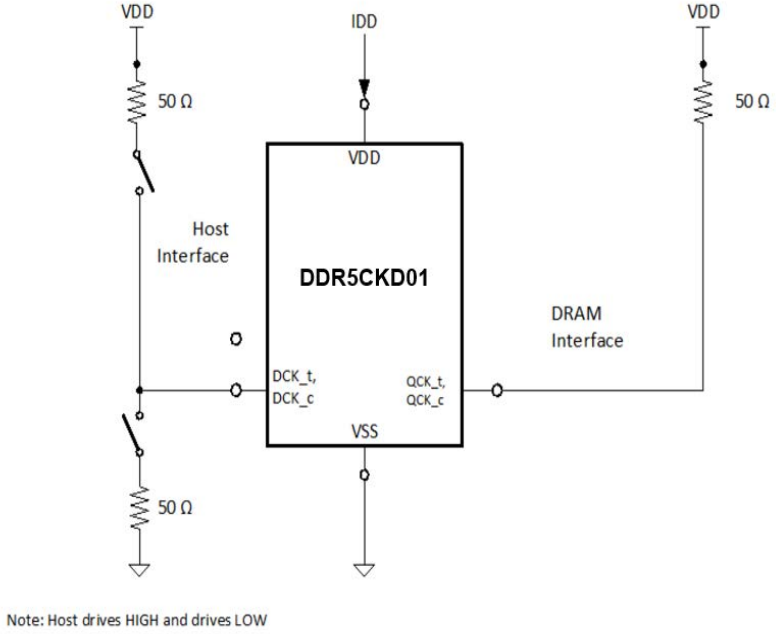


Figure 32 — Measurement Setup and Test Load for IDD Measurements

11 IDD Specification (cont'd)

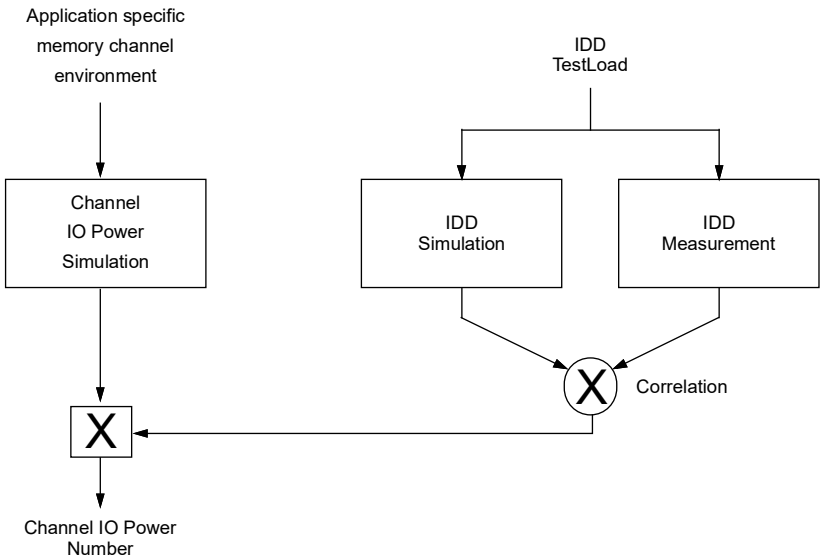


Figure 33 — Correlation from Simulated Channel IO Power to Actual Channel IO Power Supported by IDD Measurement

Table 55 — Basic IDD Measurement Conditions[1]

Symbol	Description
IDD4A	Active Current PLLOFF (PLL Bypass Mode) QCK[1:0]_[B:A]: Enabled; DCK_[B:A]_t and DCK_[B:A]_c Toggling
IDD4B	Active Current PLL ON (Single PLL MODE) QCK[1:0]_[B:A]: Enabled; DCK_A_t and DCK_A_c: Toggling
IDD4C	Active Current PLL ON (Dual PLL MODE) QCK[1:0]_[B:A]: Enabled; DCK_[B:A]_t and DCK_[B:A]_c Toggling
IDD6RA	Static Reset Current - Reset with Stable Power (PLL Bypass Mode) DRST_n: LOW; DCK_t and DCK_c: Toggling; QCK[1:0]_[B:A]: Hi-Z
IDD6RB	Static Reset Current - Reset with Stable Power (Single PLL MODE) DRST_n: LOW; DCK_t and DCK_c: Toggling; QCK[1:0]_[B:A]: Hi-Z
IDD6RC	Static Reset Current - Reset with Stable Power (Dual PLL MODE) DRST_n: LOW; DCK_t and DCK_c: Toggling; QCK[1:0]_[B:A]: Hi-Z
IDD6SB	Clock Stopped Power Down Current, PLL ON (Single PLL MODE) After Power up Initialization sequence DCK_A_t and DCK_A_c: LOW ; QCK[1:0]_[B:A]: Hi-Z
IDD6SC	Clock Stopped Power Down Current, PLL ON (Dual PLL MODE) After Power up Initialization sequence DCK_[B:A]_t and DCK_[B:A]_c: LOW ; QCK[1:0]_[B:A]: Hi-Z
NOTE 1 All tests use termination setup depicted in Figure 32.	

12 Sideband Interface

12.1 I^2C and I3C Basic Operation

At power on, by default, the CKD device comes up in I^2C mode of operation. Following applies in I^2C mode:

1. The maximum operation speed is limited to 1 MHz
2. In-band interrupts are not supported
3. Bus reset is supported.
4. Parity check is not supported except for supported CCCs.
5. Packet Error check is not supported.

The CKD device shall operate in the I^2C mode until put into I3C Basic mode via command.

The host may put the CKD device in I3C Basic mode by issuing SETAASA CCC.

Following applies in I3C mode.

1. The maximum operation speed is up to 12.5 MHz
2. In-band interrupts are supported
3. Bus reset is supported.
4. Parity check is always enabled by default.
5. Packet error check is supported and by default is disabled.

12.2 Device Interface - Protocol

System Management software in the platform can initiate system management access to the configuration registers. This can be done through Sideband Bus accesses. DDR5CKD01 components contain a Sideband Bus target port and allow access to the configuration registers.

Sideband Bus operations are made up of two major steps:

1. Writing information to registers within each component.
2. Reading configuration registers from each component.

The following sections will describe the protocol for a Sideband Bus controller to access an CKD component's internal configuration registers.

12.2.1 Serial Address of CKD Device

The 7-bit target address used for each primitive Sideband Bus transaction is determined by the 4-bit Local Device address (LID) and the 3-bit Host Device address (HID). The HID bits of the CKD device have a default value of '111' but the value of LID is determined by the ZQ Resistor value.

The 7-bit serial address of the CKD device applies to both I^2C and I3C Basic mode of operation identically.

DDR5CKD01 I2C Bus and I3C Basic Bus address:

- Target Address[6:3] = 4'b1011 (LID) if ZQCAL is connected 240 ohms, which is used for illustration within the specification.
- Target Address[6:3] = 4'b0100 (LID) if ZQCAL is connected to 480 ohms.
- Target Address[2:0] = HID code configured by SETHID command.

12.2.1 Serial Address of CKD Device (cont'd)

Table 56 — 7-bit Address of CKD Device

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	0	1	1	HID			R/W
CKD Device Type ID (LID)				Host ID (HID)			Read/ Write

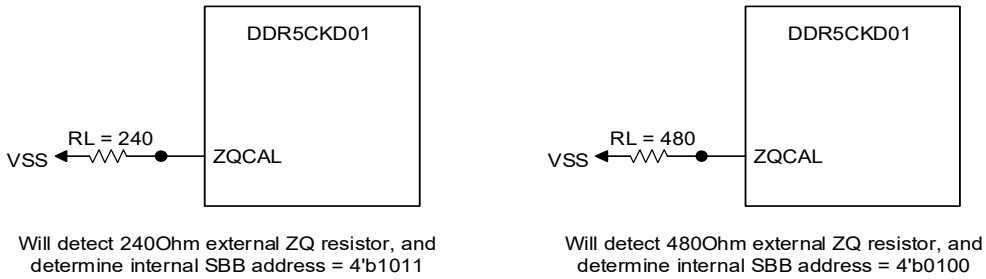


Figure 34 — ZQCAL Connection for Dual Addressing

Note: The CKD01 detects its LID during t_{INIT0}, once detection is made the device will use this address. It is sticky and only cleared upon a power cycle.

12.3 Switch from I^{2}C Mode to I3C Basic Mode

By default when CKD first powers on, it operates in I^{2}C mode. The CKD device shall operate in I^{2}C mode until put into I3C Basic mode via command.

In I^{2}C mode, the host is allowed to issue only 3 CCCs (DEVCTRL, SETHID, SETAASA). All other CCCs are not supported and the CKD device may simply ignore it. The Host must issue DEVCTRL and SETHID CCC first (if required) followed by SETAASA CCC.

The Host puts the CKD device in I3C mode by issuing SETAASA CCC.

12.4 Switch from I3C Basic Mode to I^{2}C Mode

The Host can put the CKD device back in I^{2}C mode from I3C Basic mode at any time by issuing RSTDAA CCC.

12.5 I^{2}C Target Protocol

The CKD device operates on a standard I^{2}C serial interface. Transactions where the CKD device is the targeted Target device begin with the Host issuing a START condition followed by a 7-bit CKD device address then a read or write bit, RW. All data are transmitted with the most significant bit MSB first. During the address followed by R/W bit transmission, the CKD device typically replies with an ACK unless there are exceptional conditions when it may passively assert a NACK.

The CKD device accepts 1 byte of address which covers 256 bytes of registers. The CKD device volatile register space does not require page selection process as all registers are within first 256 bytes.

12.5.1 Write Operation - Data Packet

Table 57 — Write Command Data Packet

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr[1]	1	0	1	1	HID			W=0	A	
	Address [7:0]								A	
	Data								A	
	...								A	
	Data								A	Sr or P

NOTE 1 In I^2C mode, Start or Repeat Start operation followed by 7'h7E with W=0 is only allowed for the purpose of issuing CCCs that are allowed in I^2C mode. Any other operation including another Repeat Start is considered an illegal operation.

12.5.2 Read Operation - Data Packet

Table 58 — Read Command Data Packet

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr[1]	1	0	1	1	HID			W=0	A	
	Address [7:0]								A	
Sr	1	0	1	1	HID			R=1	A[2]	
	Data								A	
	...								A	
	Data								N	Sr or P

NOTE 1 In I^2C mode, Start or Repeat Start operation followed by 7'h7E with W=0 is only allowed for the purpose of issuing CCCs that are allowed in I^2C mode. Any other operation including another Repeat Start is considered an illegal operation.

NOTE 2 If Target device NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire. CKD may eventually ACK.

12.6 I3C Basic Target Protocol

The CKD device operates on a standard I3C serial interface. Transactions where the CKD device is the targeted Target device begin with the Host issuing a START condition followed by a 7-bit CKD device address then a read or write bit, RW. All data are transmitted with the most significant bit MSB first. During the address followed by R/W bit transmission, the CKD device typically replies with an ACK unless there are exceptional conditions when it may passively assert a NACK. See Table 59. The "T" bit carries Parity information from the Host for each byte.

The Packet Error Code (PEC) function is disabled by default when the CKD device is put in I3C Basic mode. The host may optionally enable this function through DEVCTRL CCC. If enabled, the PEC is appended at the end of all transactions. If PEC is enabled, the host must complete the burst length as indicated in CMD field. In other words, the host must not interrupt the burst length prematurely for Write operation.

12.6.1 Write Operation - Data Packet

Table 59 — Write Command Data Packet; PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	0	1	1	HID			W=0	A[1,2,3]	
	Address [7:0]								T	
	Data								T	
	...								T	
	Data								T	Sr[4] or P

NOTE 1 See Figure 35 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Addr, bit [7]).
NOTE 2 The CKD NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
NOTE 3 The CKD does not check for parity error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The CKD ignores the entire packet until STOP or next Repeat Start operation.
NOTE 4 Repeat Start or Repeat Start with 7'h7E.

Table 60 — Write Command Data Packet; PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	0	1	1	HID			W=0	A[1,2,3]	
	Address [7:0]								T	
	CMD			W=0	0000				T	
	Data								T	
	...								T	
	Data								T	
	PEC								T	Sr[4] or P

NOTE 1 See Figure 35 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Addr, bit [7]).
NOTE 2 The CKD NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
NOTE 3 The CKD does not check for parity or PEC error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The CKD ignores the entire packet until STOP or next Repeat Start operation.
NOTE 4 Repeat Start or Repeat Start with 7'h7E.

The host may optionally allow CKD device to request IBI. For this case, the transactions to the CKD device begin with the I3C host issuing a START condition followed by 7'h7E and then write bit. If CKD device has a pending IBI, it transmits its 7-bit device select code followed by R=1. If CKD device has no pending IBI, there is no action taken by CKD. Table 61 and Table 62 show the I3C Basic bus write command data packet with optional IBI header for PEC disabled and PEC enabled case respectively. Note that in Table 62, PEC calculation does not include IBI header byte (7'h7E followed by W=0).

12.6.1 Write Operation - Data Packet (cont'd)

Table 61 — Write Command Data Packet with IBI Header; PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A[1,3]	
Sr	1	0	1	1	HID			W=0	A[2,3,4]	
	Address [7:0]								T	
	Data								T	
	...								T	
	Data								T	Sr[5] or P

NOTE 1 See Figure 35 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (Repeat Start)

NOTE 2 See Figure 37 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK) and See Figure to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Addr, bit [7]).

NOTE 3 The CKD NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 4 The CKD does not check for parity error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The CKD ignores the entire packet until STOP or next Repeat Start operation.

NOTE 5 Repeat Start or Repeat Start with 7'h7E.

Table 62 — Write Command Data Packet with IBI Header; PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A[1,3]	
Sr	1	0	1	1	HID			W=0	A[2,3,4]	
	Address [7:0]								T	
	CMD			W=0	0000				T	
	Data								T	
	...								T	
	Data								T	
	PEC								T	Sr[5] or P

NOTE 1 See Figure 35 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (Repeat Start)

NOTE 2 See Figure 37 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK) and See Figure to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Addr, bit [7]).

NOTE 3 The CKD NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 4 The CKD does not check for parity or PEC error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The CKD ignores the entire packet until STOP or next Repeat Start operation.

NOTE 5 Repeat Start or Repeat Start with 7'h7E.

12.6.2 Read Operation - Data Packet

The CKD device operate on a standard I3C Basic serial interface. Transactions where the CKD device is the targeted Target device begin with the Host issuing a START condition followed by a 7-bit CKD device address then a read or write bit, RW. All data are transmitted with the most significant bit MSB first. During the address followed by R/W bit transmission, the CKD device typically replies with an ACK unless there are exceptional conditions when it may passively assert a NACK. See Table 63. The "T" bit carries Parity information from the Host for each byte prior to Repeat START. After Repeat START, "T" bit carries information from CKD device to Host indicating Continuous ('1') or Stop ('0') whether it is transmitting the last byte or not.

The Packet Error Code (PEC) function is disabled by default when the CKD device is put in I3C Basic mode. The host may optionally enable this function through or DEVCTRL CCC. If enabled, the PEC is appended as shown in Table 63. If PEC is enabled, the host must complete the burst length as indicated in CMD field. In other words, the host must not interrupt the burst length pre-maturely for Read operation

Table 63 — Read Command Data Packet; PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	0	1	1	HID			W=0	A[1,2,3]	
	Address [7:0]								T	
Sr	1	0	1	1	HID			R=1	A/N[4,5]	
	Data								T=1	
	...								T=1	
	Data								T=1[6,7]	Sr[8] or P

NOTE 1 See Figure 35 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Addr, bit [7]).

NOTE 2 The CKD NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 3 The CKD does not check for parity error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The CKD ignores the entire packet until STOP or next Repeat Start operation.

NOTE 4 If Target device NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire. If Target device NACKs due to parity error in previous bytes, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity errors, the CKD may eventually ACK.

NOTE 5 See Figure 37 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).

NOTE 6 See Figure 38 to see how Host ends Target device operation.

NOTE 7 When last byte (i.e., RW255) is reached (extreme rare case), the Target device sends T = '0'. See Figure 40 to see how Target device ends the operation followed by Host STOP operation.

NOTE 8 Repeat Start or Repeat Start with 7'h7E.

12.6.2 Read Operation - Data Packet (cont'd)

Table 64 — Read Command Data Packet; PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	0	1	1	HID			W=0	A[1,2,3]	
	Address [7:0]								T	
	CMD			R=1	0000				T	
	PEC								T	
Sr	1	0	1	1	HID			R=1	A/N[4,5]	
	Data								T=1	
	...								T=1	
	Data								T=1	
	PEC								T=0[6]	Sr[7] or P

NOTE 1 See Figure 35 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Addr, bit [7]).

NOTE 2 The CKD NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 3 The CKD does not check for parity or PEC error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The CKD ignores the entire packet until STOP or next Repeat Start operation.

NOTE 4 If Target device NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire. If Target device NACKs due to PEC error or parity error in previous bytes, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity or PEC errors, the CKD may eventually ACK. The PEC calculation by the Target device only includes device select code of the ACK response of the Repeat start operation. In other words, if there are more than one Repeat Start operation, the Target device includes device select of only the last Repeat Start from the Host when it ACKs in PEC calculation and all other NACK responses of the device select code of the Repeat Start are not included in PEC calculation.

NOTE 5 See Figure 37 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).

NOTE 6 See Figure 40 to see how Target device ends the operation followed by Host STOP operation.

NOTE 7 Repeat Start or Repeat Start with 7'h7E.

The host may optionally allow CKD device to request IBI. For this case, the transactions to the CKD device begin with the I3C Basic host issuing a START condition followed by 7'h7E and then write bit. If CKD device has a pending IBI, it transmits its 7-bit device select code followed by R=1. If CKD device has no pending IBI, there is no action taken by CKD. Table 61 and Table 62 show the I3C Basic bus write command data packet with optional IBI header for PEC disabled and PEC enabled case respectively. Note that in Table 62, PEC calculation does not include IBI header byte (7'h7E followed by W=0)

12.6.2 Read Operation - Data Packet (cont'd)

Table 65 — Read Command Data Packet with IBI Header; PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A[1,3]	
Sr	1	0	1	1	HID			W=0	A[2,3,4]	
	Address [7:0]								T	
Sr	1	0	1	1	HID			R=1	A/N[5,6]	
	Data								T=1	
	...								T=1	
	Data								T=1[7,8]	Sr[9] or P

NOTE 1 See Figure 35 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (Repeat Start)

NOTE 2 See Figure 37 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK) and see Figure 35 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Addr, bit [7]).

NOTE 3 The CKD NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 4 The CKD does not check for parity error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The CKD ignores the entire packet until STOP or next Repeat Start operation.

NOTE 5 See Figure 37 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).

NOTE 6 If Target device NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire. If Target device NACKs due to parity error in previous bytes, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity errors, CKD may eventually ACK.

NOTE 7 See Figure 39 to see how Host ends Target device operation.

NOTE 8 When last byte (i.e., RW255) is reached (extreme rare case), the Target device sends T = '0'. See Figure 40 to see how Target device ends the operation followed by Host STOP operation.

NOTE 9 Repeat Start or Repeat Start with 7'h7E.

12.6.2 Read Operation - Data Packet (cont'd)

Table 66 — Read Command Data Packet with IBI Header; PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A[1,3]	
Sr	1	0	1	1	HID			W=0	A[2,3,4]	
	Address [7:0]								T	
	CMD			R=1	0000				T	
	PEC								T	
Sr	1	0	1	1	HID			R=1	A/N[5,6]	
	Data								T=1	
	...								T=1	
	Data								T=1	
	PEC								T=0[7]	Sr[8] or P

NOTE 1 See Figure 35 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (Repeat Start).

NOTE 2 See Figure 37 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK) and see Figure 35 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Addr, bit [7]).

NOTE 3 The CKD NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 4 The CKD does not check for parity or PEC error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The CKD ignores the entire packet until STOP or next Repeat Start operation.

NOTE 5 See Figure 37 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).

NOTE 6 If Target device NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire. If Target device NACKs due to PEC error or parity error in previous bytes, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity or PEC errors, the CKD may eventually ACK. The PEC calculation by the Target device only includes device select code of the ACK response of the Repeat start operation. In other words, if there are more than one Repeat Start operation, the Target device includes device select of only the last Repeat Start from the Host when it ACKs in PEC calculation and all other NACK responses of the device select code of the Repeat Start are not included in PEC calculation.

NOTE 7 See Figure 40 to see how Target device ends the operation followed by Host STOP operation.

NOTE 8 Repeat Start or Repeat Start with 7'h7E.

12.6.2 Read Operation - Data Packet (cont'd)

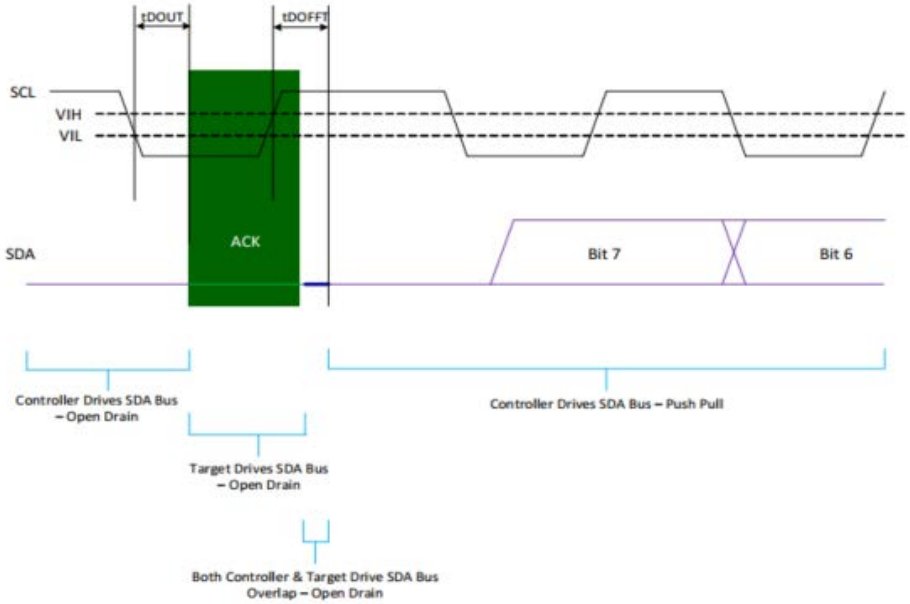


Figure 35 — Target Open Drain to Host Push Pull Hand Off Operation

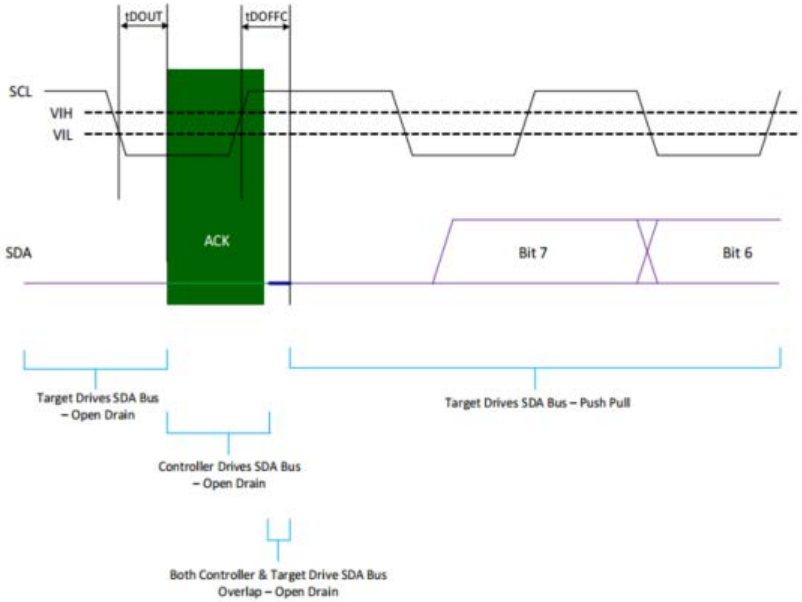


Figure 36 — Controller Open Drain (ACK) to Target Push Pull Hand Off Operation

12.6.2 Read Operation - Data Packet (cont'd)

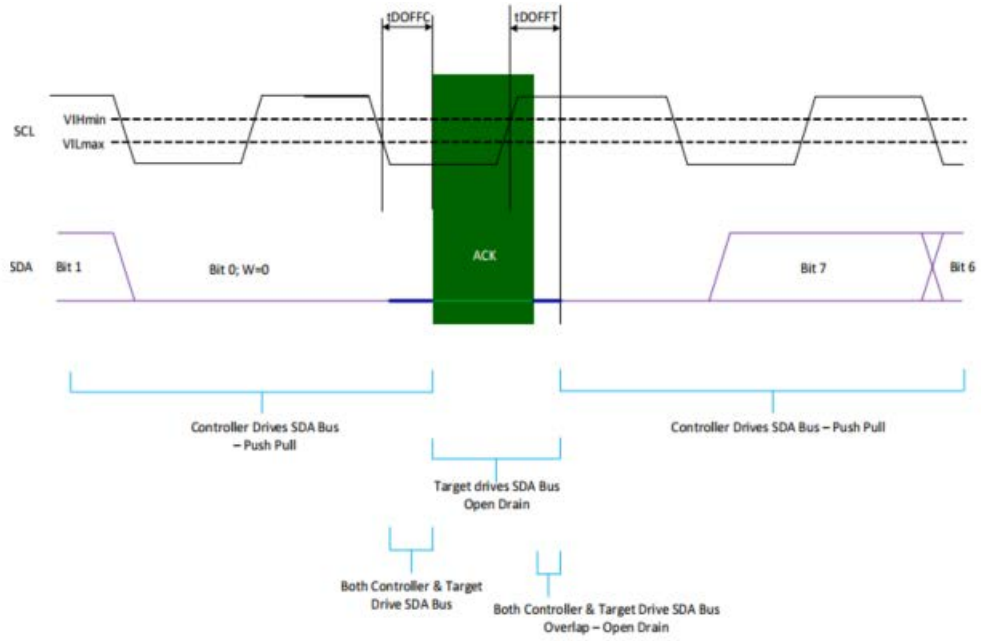


Figure 37 — Controller Push Pull to Target Open Drain Hand Off Operation (Write)

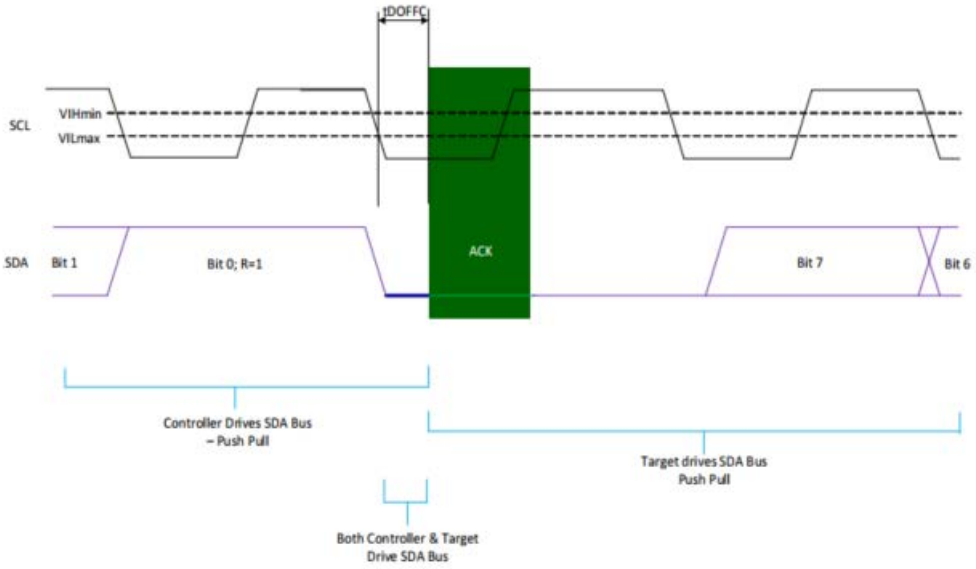


Figure 38 — Controller Push Pull to Target Open Drain Hand Off Operation (Read)

12.6.2 Read Operation - Data Packet (cont'd)

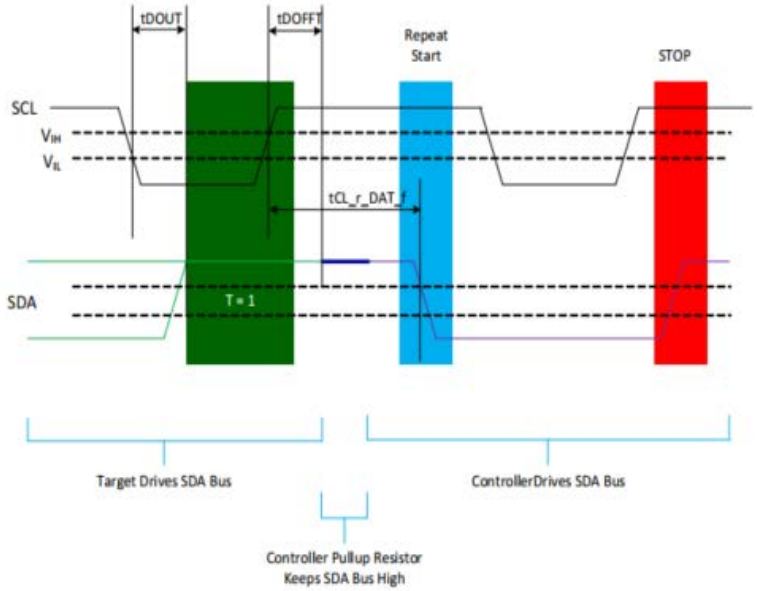


Figure 39 — T=1; Host Ends Read with Repeated START and STOP Waveform

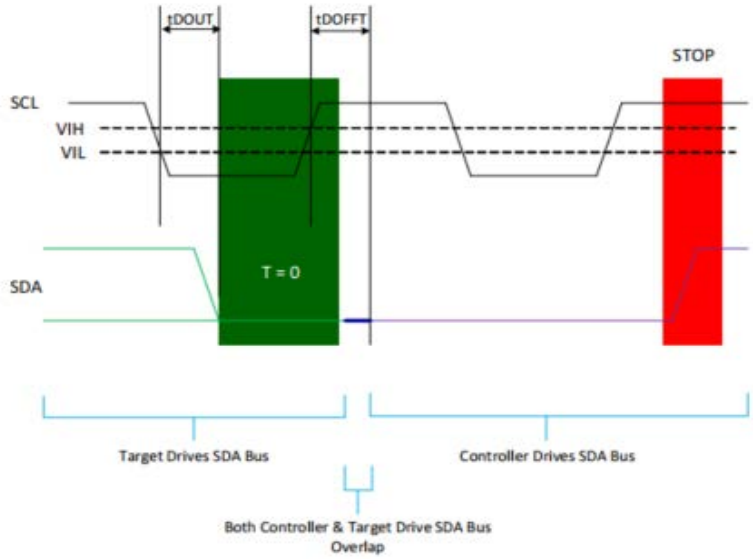


Figure 40 — T=0; Target Ends Read; Controller Generates STOP

12.7 In Band Interrupt (IBI)

In-Band interrupts may be generated by the CKD device if IBI is enabled by receiving a broadcast or directed ENEC CCC. In I^2C mode, in-band interrupt function is not supported. Only I3C Basic mode supports the in-band interrupt function.

12.7.1 Enabling/Disabling In-Band Event Interrupts

By default, all interrupt sources are disabled (i.e., set to '0'). The host may enable interrupts in the CKD device. Once enabled, the CKD device sends an IBI when that event occurs.

1. When any of the bits in RW28[1:0] (Parity Error or PEC Error Status Bits) get set to '1', the CKD device sets RW28[7] (In-band Interrupt Status) to 1 and updates Pending Interrupt Bits [3:0] = '0001' for GETSTATUS CCC.
   a. If IBI is enabled by ENEC CCC, the CKD device sends the IBI at next available opportunity.
   b. If IBI is disabled by DISEC CCC, the device does not send the IBI regardless of the register bit status in RW28.

12.7.2 Mechanics of Interrupt Generation

Event interrupts may be generated by the local device if IBI is enabled. When there is a pending interrupt (i.e., RW28 [7] = '1') and if IBI is enabled the CKD device requests an interrupt after detecting START condition by transmitting its 7-bit binary address (LID bits followed by HID bits) followed by R/W = '1' on the SDA bus serially (synchronized by SCL falling transitions).

If CKD device detects no START condition but if the I3C bus (SDA and SCL) has been inactive (no edges seen) for t_{AVAL} period, then CKD device may assert SDA low by t_{IBI_ISSUE} time to request an interrupt. When the CKD device requests an interrupt, the Host toggles the SCL. The CKD device transmits its 7-bit binary address (LID bits followed by HID bits) followed by R/W bit = '1' to the Host.

When the CKD device requests an interrupt, the host may take one of the two actions below.

- The Host sends ACK on 9th bit to accept the interrupt request. At this point, if the CKD device confirms that it has won the arbitration, the CKD device transmits the IBI payload as shown in Table 67 and Table 68 for PEC disabled and PEC enabled configuration respectively. See Figure 41. Figure 41 just shows only first two data bits of the MDB byte to illustrate the timing. The interrupt payload contains MDB followed by RW28. The host then issues the STOP command. Note the timing waveform in Figure 41. The host then accepts the IBI payload if it sends an ACK on 9th bit to accept the interrupt request. The host can interrupt the IBI payload at T bit. If host stops the IBI payload at T bit in the middle of payload, the CKD retains the IBI status flag RW28[7] and Pending Interrupt Bits [3:0] internally and waits for the next opportunity to request an interrupt. If the CKD device successfully transmits the entire IBI payload, it then clears IBI status flag and Pending Interrupt Bits [3:0] = '0000' on its own and does not request for an IBI again unless there is another different event occurs; for another same event, the device does not request for an IBI.
- The Host sends NACK on the 9th bit as shown in Figure 42 followed by a STOP command. In this case, the CKD device does not transmit the IBI payload and waits for the next opportunity to request an interrupt. At this point, though Host sent an NACK, it does have a knowledge of which local device sent the IBI request. The CKD device retains the IBI status flag RW28[7] and Pending Interrupt Bits [3:0] = '0001'

12.7.2 Mechanics of Interrupt Generation (cont'd)

Table 67 — Target Device IBI Payload Packet; PEC is Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/T	Stop
S	1	0	1	1	HID			R=1	A[1]	
	MDB = 0x00								T=1	
	RW28								T=0[2]	P

NOTE 1 See Figure 36 to see how the transition occurs from Host Open Drain (ACK) to Target Push Pull Operation (1st bit of MDB Byte bit [7]).
NOTE 2 See Figure 40 to see how Target device ends the operation followed by Host STOP operation.

Table 68 — Target Device IBI Payload Packet; PEC is Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/T	Stop
S	1	0	1	1	HID			R=1	A[1]	
	MDB 0x00								T=1	
	RW28								T=1	
	PEC								T=0[2]	P

NOTE 1 See Figure 36 to see how the transition occurs from Host Open Drain (ACK) to Target Push Pull Operation (1st bit of MDB Byte bit [7]).
NOTE 2 See Figure 40 to see how Target device ends the operation followed by Host STOP operation.

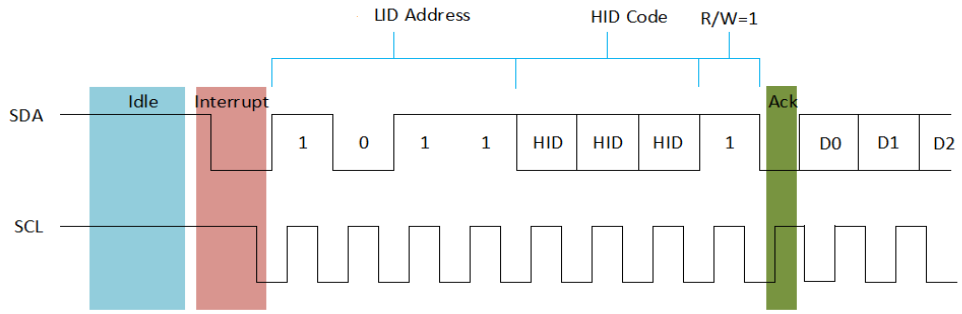


Figure 41 — CKD Requests Interrupt, Host Ack followed by CKD Device IBI Payload

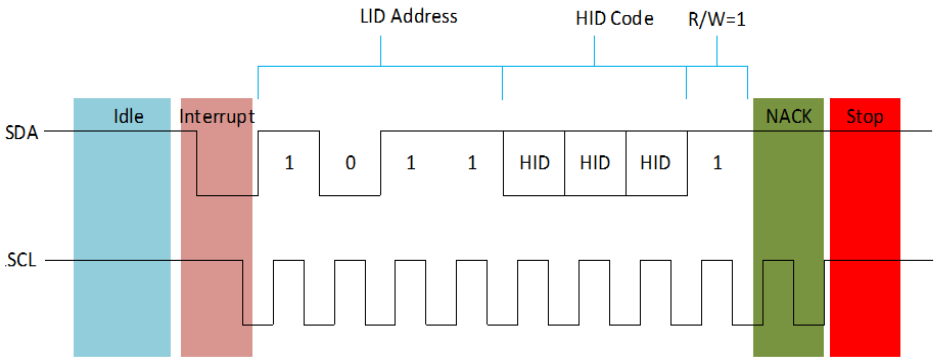


Figure 42 — CKD Requests Interrupt; Host NACK followed by STOP

12.7.3 Interrupt Arbitration

As there are multiple devices in the I3C Basic bus, more than one device may request an interrupt when the Host I3C Basic bus is inactive for t_{AVAL} period. This makes an arbitration process necessary.

There could be up to 13 different devices, including the CKD, in the I3C Basic bus of a DDR5 DIMM application environment.

On a typical DDR5 DIMM application environment, all devices behind the SPD5 Hub device have the same 3-bit HID code. Hence, the arbitration is always won by the lowest 4-bit LID code. For example, if one local target device has LID code of '0010' and other device (CKD) has a LID code of '1011', through the arbitration process, the LID code of '0010' wins. If a higher priority device than the CKD device is serviced, the CKD must release the bus and wait for the next opportunity to request an interrupt.

It is possible for the Controller to start a command transaction at the same time as the CKD requests an interrupt. When this happens, the Controller participates in the arbitration process along with the other devices in the bus. During the arbitration phase, there will always be only one winning device and it could be one of the target devices (e.g., CKD) or the Controller. If the Controller wins during the arbitration phase, it continues with normal operation. The losing devices (e.g., CKD) must wait for next opportunity to send an interrupt. If the Controller loses the arbitration, it must let go of the bus. When the Controller loses during the arbitration, it must allow the winning device (e.g., CKD) to finish sending its 4-bit LID code followed by the 3-bit HID code followed by R/W = '1'. At this point, during the 9th bit, the Controller has the following two options:

- Option 1. The Controller sends ACK to accept the interrupt and hence accepts the IBI payload from the winning device (e.g., CKD). After the IBI payload, the Controller issues a STOP operation.
- Option 2. Host sends NACK followed by STOP operation.

In cases when the Controller is starting a command transaction to an CKD that is requesting an interrupt at the same time, neither the Controller or the CKD know if they are a winner until the 8th bit, and Controller always wins. This is because the CKD sends R/W=1 (8th bit) during the interrupt. The Controller sets R/W=0 (8th bit) during the operation. As a result, the Controller wins and the CKD must let go of the bus and wait for the next opportunity to send an interrupt.

12.7.4 Clearing Status Registers

The CKD device provides the device status in RW28. When the CKD device generates an IBI condition in RW28[1:0], it sets RW28[7] to '1'. The CKD clears RW28[7] to '0' automatically when it sends a complete IBI (including payload and without interruption) the operation gets an ACK from the host. The status information in RW28[1:0] are latched and remains valid even after target device sends payload or if the condition that triggered to generate the status is no longer present. The host must explicitly clear the status register through Clear command by writing '1' to register bits in RW29[1:0]. After the Host Clear command, if the condition is still present, the device will again set the status information in RW28 registers appropriately and will again generate interrupt at next available opportunity. When RW28[1:0] are cleared to '00' as a result of a Clear command in RW29, the IBI Status Register RW28[7] will also get cleared to '0' by the CKD hardware. IBI will get disabled when the CKD receives DISEC CCC. IBI may also get disabled when the CKD receives RSTDAA CCC since the host is expected to disable Error Interrupts by issuing DISEC CCC prior to sending the RSTDAA CCC.

12.8 Packet Error Check (PEC) Function

In I^2C mode, packet error checking is not supported. Only I3C Basic mode supports packet error checking.

The CKD device implement an 8-bit Packet Error Code (PEC) which is appended at the end of all transactions if PECs is enabled through DEVCTRL CCC. The PEC is a CRC-8 value calculated on all the messages bytes except for START, STOP, REPEATED START conditions or T-bits, ACK and NACK and IBI header (7'h7E followed W=0) bits.

12.8 Packet Error Check (PEC) Function (cont'd)

The polynomial for CRC-8 calculations is:

- $C(X) = X^8 + X^2 + X^1 + 1$

The seed value for PEC function is all zero.

When Host calculates PEC for CKD device, it includes LID and HID bits followed by R/W bit.

12.9 Parity Error Check Function

In I^2C mode, parity error checking is not supported except for supported CCCs. Only I3C mode supports parity error checking.

By default, when CKD device is put in I3C mode, parity function is automatically enabled. The host can disable the function after it is enabled. Host can also disable the parity function with DEVCTRL CCC. When parity function is disabled, the CKD device simply ignores the "T" bit information from the Host. The host may actually choose to compute the parity and send that information during "T" bit or simply drive static low or high in "T" bit.

The CKD device implements ODD parity. If an odd number of bits in the byte are '1', the parity bit value is '0'. If even number of bits in the byte are '1', the parity bit value is '1'. The host computes the parity and sends during "T" bit.

12.10 Packet Error Check and Parity Error Handling

There are two types of error checking done by the CKD device. Parity error checking and Packet Error checking. By default, the parity error checking is always enabled and packet error checking is disabled. The host may enable the packet error checking at any time. The parity error is checked for each byte in a packet except for the device select code byte from the host. The host sends parity error information in "T" bit.

I3C basic defines S0, S1, S2, S3, S4, S5, S6 error detection for Target devices. Only S1 and S2 error detection is supported by the CKD for parity checking. All other errors are not supported and not applicable.

12.10.1 Write Command Data Packet Error Handling - PEC Disabled

The CKD device checks for the parity error for each byte in a packet that it receives from the host except for the device select code byte that it receives from the host.

Table 69 — Write Command Data Packet; PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	0	1	1	HID			W=0	A[1,2,3]	
	Address [7:0]								T	
	Data								T	
	...								T	
	Data								T	Sr[4] or P

NOTE 1 See Figure 36 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Addr, bit [7]).
NOTE 2 The CKD NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
NOTE 3 The CKD does not check for parity error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The CKD ignores the entire packet until STOP or next Repeat Start operation.
NOTE 4 Repeat Start or Repeat Start with 7'h7E.

Write command - if no parity error:

- The CKD device executes the command.

Write command - if parity error:

- The CKD device discards the byte in the packet that had a parity error.
- The CKD device discards all subsequent bytes in that packet until the STOP operation. The CKD device may or may not check parity for all sub-sequent bytes in that packet.
- Note that as the packet contains more than one byte, if first byte had no parity error but the second byte had a parity error, the CKD device may or may not execute the first byte operation but second byte and all subsequent bytes operations are discarded.
- The CKD device sets the RW28[0] and RW28[7] and P_Err in GETSTATUS CCC to '1'; updates Pending Interrupt Bits [3:0] in GETSTATUS CCC to '0001' and waits for the next opportunity to send an in band interrupt if IBI is enabled.

12.10.2 Read Command Data Packet Error Handling - PEC Disabled

The CKD device checks for parity error for each byte in a packet except for the device select code byte that it receives from the host prior to Repeat Start as shown in Table 70.

The CKD device does not compute the parity when it sends the data to the Host. The Host does not check for parity error for the bytes shown in Table 70. The device sends Continuous ('1') or Stop ('0') information during "T" bit when CKD device is sending the read data.

Table 70 — Read Command Data Packet; PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	0	1	1	HID			W=0	A[1,2,3]	
	Address [7:0]								T	
Sr	1	0	1	1	HID			R=1	A/N[4,5]	
	Data								T=1	
	...								T=1	
	Data								T=1[6,7]	Sr[8] or P

NOTE 1 See Figure 35 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Addr, bit [7]).
NOTE 2 The CKD NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
NOTE 3 The CKD does not check for parity error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The CKD ignores the entire packet until STOP or next Repeat Start operation.
NOTE 4 If Target device NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire. If Target device NACKs due to parity error in previous bytes, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity errors, CKD may eventually ACK.
NOTE 5 See Figure 37 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).
NOTE 6 See Figure 39 to see how Host ends Target device operation.
NOTE 7 When last byte (i.e., MR255) is reached (extreme rare case), the Target device sends T = '0'. See Figure 40 to see how Target device ends the operation followed by Host STOP operation.
NOTE 8 Repeat Start or Repeat Start with 7'h7E.

Read Command - If no parity error:

- The CKD sends ACK back to the host when Host perform Start Repeat operation.
- The CKD device executes the command and sends the data as shown in Table 70.

Read Command - If parity error:

- The CKD device discards the byte in the packet that had a parity error.
- The CKD device sends NACK back to the host when Host performs a Start Repeat operation. This is shown in the RED color cell in Table 70. The NACK represents either a parity error or that CKD is not able to start the read operation. The host may re-try Repeat Start again. The host may do the Repeat Start as many times as it may desire. If the CKD Target device NACKs due to parity error in a previous byte from the host, it will always NACK regardless of how many times Host tries Repeat Start.
- The CKD does not send the data shown in Table 70 and instead expects Host to perform STOP operation.
- The CKD device sets RW28[0] and RW28[7], and P_Err in GETSTATUS CCC to '1'; updates Pending Interrupt Bits [3:0] in GETSTATUS CCC to '0001' and waits for the next opportunity to send an in band interrupt if IBI is enabled.

12.10.3 Write Command Data Packet Error Handling - PEC Is Enabled

The CKD device checks for the parity error for each byte in a packet that it receives from the host except for the device select code byte that it receives from the host as shown in Table 71. Further, the CKD device checks for the packet error for the entire packet (from Start condition until last byte of Data) that it receives from the host as shown in Table 71.

Table 71 — Write Command Data Packet; PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	0	1	1	HID			W=0	A[1,2,3]	
	Address [7:0]								T	
	CMD			W=0	0	0	0	0	T	
	Data								T	
	...								T	
	Data								T	
	PEC								T	Sr[4] or P

NOTE 1 See Figure 35 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Addr, bit [7]).
NOTE 2 The CKD NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
NOTE 3 The CKD does not check for parity or PEC error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The CKD ignores the entire packet until STOP or next Repeat Start operation.
NOTE 4 Repeat Start or Repeat Start with 7'h7E.

Write command - if no parity error:

- The CKD device waits for the entire packet. If no error in packet, the CKD device executes the command. If there is an error in the packet, the CKD device discards the entire packet and does not execute that packet and waits for STOP; sets the RW28[1]and RW28[7] and PEC_Err in GETSTATUS CCC to '1';updates Pending Interrupt Bits [3:0] in GETSTATUS CCC to '0001' and waits for the next opportunity to send in band interrupt if IBI is enabled.

Write command - if parity error:

- The CKD device discards that byte and the entire packet until STOP operation.
- The CKD device sets RW28[0] and RW28[7] and P_Err in GETSTATUS CCC to '1'; updates Pending Interrupt Bits [3:0] in GETSTATUS CCC to '0001' and waits for the next opportunity to send in band interrupt if IBI is enabled.
- The CKD device may or may not check the error for the packet. If the CKD device checks for the packet error, likely it will detect an error in the packet and the device may also set RW28[1] and PEC_Err in GETSTATUS CCC to '1' as well.

12.10.4 Read Command Data Packet Error Handling - PEC Is Enabled

The CKD device checks for parity error for each byte in a packet except for the device select code byte that it receives from the host prior to Repeat Start as shown in Table 72.

The CKD device does not compute the parity when it sends the data to the Host. The does not check for parity error for the bytes shown in Table 72. The device sends Continuous ('1') or Stop ('0') information during "T" bit when CKD device is sending the read data.

12.10.4 Read Command Data Packet Error Handling - PEC Is Enabled (cont'd)

The CKD device checks for the PEC error in a packet that it receives from Host from Start condition to Repeat Start (from first device select code followed by the address offset and CMD byte).

The CKD device computes the packet error code for the entire packet starting with Repeat Start (device select code and the data CKD device transmits back to Host).

Table 72 — Read Command Data Packet; PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	0	1	1	HID			W=0	A[1,2,3]	
	Address [7:0]								T	
	CMD			R=1	0	0	0	0	T	
	PEC								T	
Sr	1	0	1	1	HID			R=1	A/N[4,5]	
	Data								T=1	
	...								T=1	
	Data								T=1	
	PEC								T=0[6]	Sr[7] or P

NOTE 1 See Figure 35 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Addr, bit [7]).

NOTE 2 The CKD NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 3 The CKD does not check for parity or PEC error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The CKD ignores the entire packet until STOP or next Repeat Start operation.

NOTE 4 If Target device NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire. If Target device NACKs due to PEC error or parity error in previous bytes, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity or PEC errors, CKD may eventually ACK. The PEC calculation by the Target device only includes device select code of the ACK response of the Repeat start operation. In other words, if there are more than one Repeat Start operation, the Target device includes device select of only the last Repeat Start from the Host when it ACKs in PEC calculation and all other NACK responses of the device select code of the Repeat Start are not included in PEC calculation.

NOTE 5 See Figure 38 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).

NOTE 6 See Figure 40 to see how Target device ends the operation followed by Host STOP operation.

NOTE 7 Repeat Start or Repeat Start with 7'h7E.

Read command - If no parity error and no PEC error

- The CKD device sends ACK back to the host when Host perform a Start Repeat operation.
- The CKD device executes the command and sends the data as shown in Table 72.
- The CKD computes PEC for the bytes (from Start condition to PEC byte prior to Repeat Start) shown in the cells in Table 72.

Read command - if parity error or PEC error

- The CKD device discards the byte in the packet that had a parity error.
- The CKD device discards second byte in that packet if a parity error occurred in first byte. The CKD device may or may not check parity for the second byte in that packet.
- The CKD device discards the packet if there is a PEC error.
- The CKD sends NACK back to the host when Host perform Start Repeat operation. This is shown in the RED color cell in Table 72. The NACK represents either PEC error or a parity error in one of the three bytes or that CKD is not able to start the read operation. The host may retry Repeat Start again. The host may do the Repeat Start as many times it may desire.

12.10.4 Read Command Data Packet Error Handling - PEC Is Enabled (cont'd)

The PEC calculation by CKD device only includes device select code of the ACK responses of the Repeat Start operation. In other words, if there are more than one Repeat Start operation, the CKD device includes the device select of only the last Repeat Start from the Host when it ACKs in PEC calculation and other NACK responses of the device select codes of the Repeat Start are not included in PEC calculation. If the CKD Target device NACKs due to PEC error or a parity error in a previous bytes from Host, it will always NACK regardless of how many times Host tries Repeat Start.

- The CKD device does not send any data shown in Table 72 and instead expects Host to perform STOP operation.
- The CKD device sets RW28[0] and RW28[7] and P_Err in GETSTATUS CCC to '1' for parity error and RW28[1] and PEC_Err in GETSTATUS CCC to '1' for PEC error. Further, CKD updates Pending Interrupt Bits [3:0] in GETSTATUS CCC to '0001' and waits for the next opportunity to send an in band interrupt if IBI is enabled.

12.11 CCC Packet Error Handling

Parity error and PEC error detected in a CCC packet are handled the same way as described for normal Read/Write operations.

12.11.1 Error Reporting

All error conditions detected by the CKD devices are captured in RW28.Section 12.12

There are three different possible ways error information can be communicated to the host.

1. The host makes the read request to RW28
2. The host starts any transactions with 7'h7E IBI header (Only applicable in I3C mode).
3. The CKD device sends in band interrupt if enabled, when its SCL and SDA input has been idle for t_{AVAL} time (Only applicable in I3C Basic mode).

12.12 I3C Basic Common Command Codes (CCC)

The I3C Basic spec lists large number of Common Command Codes (CCC). Not all CCC are required to be supported. The CKD device NACKs for all unsupported CCC. The CKD supports CCC as listed in Table 73.

The CKD device requires STOP operation in between when switching from CCC operation to private device specific Write or Read operation and vice versa. In other words, any CCC operation must be followed by STOP operation before continuing to any device specific Write or Read. Similarly, any device specific Write or Read operation must be followed by STOP operation before continuing to any CCC operation. The CKD device also requires STOP operation from any direct CCC to broadcast CCC.

The CKD device does allow Repeat Start operation from between any direct CCC to any other direct CCC or between any broadcast CCC to any other broadcast CCC or between any private targeted Write or Read to a single device.

12.12 I3C Basic Common Command Codes (CCC) (cont'd)

Table 73 — CKD CCC Support Requirement

CCC	Mode	Code	Description	Note
ENEC	Broadcast	0x00	Enable Event Interrupts	
	Direct	0x80		
DISEC	Broadcast	0x01	Disable Event Interrupts	
	Direct	0x81		
RSTDAA	Broadcast	0x06	Put the device in I^2C Mode (aka: Reset Dynamic Address Assignment)	
SETAASA	Broadcast	0x29	Put the device in I3C Basic Mode (aka: Set All Addresses to Static Address)	
GETSTATUS	Direct	0x90	Get Device Status	
DEVCAP	Direct	0xE0	Get Device Capability	1
SETHID	Broadcast	0x61	CKD updates 3-bit HID field	1
DEVCTRL	Broadcast	0x62	Configure SPD Hub and all devices behind Hub	1
NOTE 1 JEDEC specific CCC.				

12.12.1 ENEC CCC

The ENEC CCC is only supported after device is put in I3C Basic mode. In I^2C mode, it is illegal for host to issue this CCC. When ENEC CCC is registered by the CKD, it updates internally and it takes in effect at the next Start operation (i.e., after STOP condition). Table 74 to Table 77 shows an example of a single ENEC CCC. Table 78 shows the encoding definition for ENEC CCC.

If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W=0 byte in PEC calculation.

Table 74 — ENEC CCC - Broadcast

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A[1]	
	0x00 (Broadcast)								T	
	0x00							ENINT	T	Sr[2] or P
NOTE 1 The CKD NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start. NOTE 2 Repeat Start or Repeat Start with 7'h7E.										

Table 75 — ENEC CCC - Broadcast with PEC

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A[1]	
	0x00 (Broadcast)								T	
	0x00							ENINT	T	
	PEC								T	Sr[2] or P
NOTE 1 The CKD NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start. NOTE 2 Repeat Start or Repeat Start with 7'h7E.										

12.12.1 ENEC CCC (cont'd)

Table 76 — ENEC CCC - Direct

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A[1]	
	0x80 (Direct)								T	
Sr	DevID[6:0]							W=0	A	
	0x00							ENINT	T	Sr[2] or P

NOTE 1 The CKD NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
NOTE 2 Repeat Start or Repeat Start with 7'h7E.

Table 77 — ENEC CCC - Direct with PEC

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A[1]	
	0x80 (Direct)								T	
	PEC								T	
Sr	DevID[6:0]							W=0	A	
	0x00							ENINT	T	
	PEC								T	Sr[2] or P

NOTE 1 The CKD NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
NOTE 2 Repeat Start or Repeat Start with 7'h7E.

Table 78 — ENEC CCC Byte Encoding

Bit	Encoding	Notes
ENINT	0 = No Action 1 = Enable IBI Interrupt	It is illegal for Host to issue ENEC CCC with ENINT bit = '0'

12.12.2 DISEC CCC

The DISEC CCC is only supported after device is put in I3C Basic mode. In I^2C mode, it is illegal for host to issue this CCC. When DISEC CCC is registered by the CKD, it updates internally and it takes in effect at the next Start operation (i.e., after STOP condition). Table 79 to Table 82 shows an example of a single DISEC CCC. Table 83 shows the encoding definition for DISEC CCC.

If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W=0 byte in PEC calculation

12.12.2 DISEC CCC (cont'd)

Table 79 — DISEC CCC - Broadcast

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A[1]	
	0x01 (Broadcast)								T	
	7'h00							DISINT	T	Sr[2] or P

NOTE 1 The CKD NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
NOTE 2 Repeat Start or Repeat Start with 7'h7E.

Table 80 — DISEC CCC - Broadcast with PEC

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A[1]	
	0x01 (Broadcast)								T	
	7'h00							DISINT	T	
	PEC								T	Sr[2] or P

NOTE 1 The CKD NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
NOTE 2 Repeat Start or Repeat Start with 7'h7E.

Table 81 — DISEC CCC - Direct

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A[1]	
	0x81 (Direct)								T	
Sr	DevID[6:0]							W=0	A	
	0x00							DISINT	T	Sr[2] or P

NOTE 1 The CKD NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
NOTE 2 Repeat Start or Repeat Start with 7'h7E.

Table 82 — DISEC CCC - Direct with PEC

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A[1]	
	0x81 (Direct)								T	
	PEC								T	
Sr	DevID[6:0]							W=0	A	
	0x00							DISINT	T	
	PEC								T	Sr[2] or P

NOTE 1 The CKD NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
NOTE 2 Repeat Start or Repeat Start with 7'h7E.

12.12.2 DISEC CCC (cont'd)

Table 83 — DISEC CCC Byte Encoding

Bit	Encoding	Notes
DISINT	0 = No Action 1 = Disable IBI Interrupt	It is illegal for Host to issue DISEC CCC with DISINT bit = '0'

12.12.3 RSTDAA CCC

The RSTDAA CCC is only supported after device is put in I3C Basic mode. In I^2C mode, this CCC is ignored. When RSTDAA CCC is registered by the CKD, it updates internally and it takes in effect at the next Start operation (i.e., after STOP condition). Further it internally disables IBI and PEC functions, enables Parity Error function.

Table 84 and Table 85 show an examples of a single RSTDAA CCC.

If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W=0 byte in PEC calculation.

Table 84 — RSTDAA CCC - Broadcast

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A[1]	
	0x06 (Broadcast)								T	Sr[2] or P

NOTE 1 The CKD NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
NOTE 2 Repeat Start or Repeat Start with 7'h7E.

Table 85 — RSTDAA CCC - Broadcast with PEC

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A[1]	
	0x06 (Broadcast)								T	
	PEC								T	Sr[2] or P

NOTE 1 The CKD NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
NOTE 2 Repeat Start or Repeat Start with 7'h7E.

12.12.4 SETAASA CCC

The SETAASA CCC is only supported when device is in I^2C mode. In I^2C mode, when host issues CCC, to guarantee that this CCC is registered by the device without any error, the host shall limit the maximum speed operation for this CCC to 1 MHz. In I3C Basic mode, this CCC is ignored. When SETAASA CCC is registered by the CKD, it updates internally and it takes in effect at the next Start operation (i.e., after STOP condition). Table 86 shows an example of a single SETAASA CCC.

SETAASA CCC does not support PEC function as device is in I^2C mode and there is no PEC function in I^2C mode.

12.12.4 SETAASA CCC (cont'd)

Table 86 — SETAASA CCC - Broadcast

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A	
	0x29 (Broadcast)								T	P

12.12.5 GETSTATUS CCC

The GETSTATUS CCC is supported in I3C Basic mode. In I^2C mode, this CCC is ignored (i.e., it is not executed internally and GETSTATUS CCC code is not acknowledged and host must do STOP operation). Table 87 to Table 88 show an example of a single GETSTATUS CCC.

If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W=0 byte in PEC calculation.

Table 87 — GETSTATUS CCC - Direct

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A[1]	
	0x90 (Direct)								T	
Sr	DevID[6:0]							R=1	A	
	PEC_Err	0	0	0	0	0	0	0	T	
	0	0	P_Err	0	Pending Interrupt				T	Sr[2] or P

NOTE 1 The CKD NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
NOTE 2 Repeat Start or Repeat Start with 7'h7E.

Table 88 — GETSTATUS CCC - Direct with PEC[1]

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A[2]	
	0x90 (Direct)								T	
	PEC								T	
Sr	DevID[6:0]							R=1	A	
	PEC_Err	0	0	0	0	0	0	0	T	
	0	0	P_Err	0	Pending Interrupt				T	
	PEC								T	Sr[3] or P

NOTE 1 GETSTATUS CCC with PEC check is only supported in I3C Basic mode.
NOTE 2 The CKD NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
NOTE 3 Repeat Start or Repeat Start with 7'h7E.

12.12.5 GETSTATUS CCC (cont'd)

Table 89 — GETSTATUS MSb-LSb Format

Bits	Field	Description
15	PEC Error	DDR5CKD01 returns the value of RW28[1]. This bit is cleared when Host issues Clear Command to RW29[1]. 0 = No Error 1 = PEC Error Occurred
14:8	Vendor Reserved	Hard coded to all-zeros in DDR5CKD01.
7:6	Activity Mode	Hard coded to all-zeros in DDR5CKD01.
5	Protocol Error	DDR5CKD01 returns the value of RW28[0]. This bit is cleared when Host issues Clear Command to RW29[0]. 0 = No Error 1 = Protocol Error; Parity Error Occurred
4	Reserved	Hard coded to zero in DDR5CKD01.
3:0	Pending Interrupt	DDR5CKD01 returns the value of RW28[7] in Bit 0. Bit 0 is cleared when Host issues a Clear Command that causes the IBI Status register RW28[7] to get cleared. 0000 = No Pending Interrupt 0001 = Pending Interrupt All other encodings are reserved

When the CKD device responds to GETSTATUS CCC, after it completes the response, the PEC_Err, P_Err and Pending Interrupt Bits [3:0] do not automatically get cleared. The host must explicitly clear the appropriate status register through Clear command by writing '1' to corresponding register or by issuing Global Clear command. Once the CKD device clears the appropriate status register, only then PEC_Err, P_err and Pending Interrupt Bits [3:0] gets cleared.

After host issues clear command, if the condition is still present, the device will again set the appropriate status register, sets the IBI status register to '1' and Pending Interrupt Bits [3:0] to '0001'.

12.12.6 DEVCAP CCC

The DEVCAP CCC is only supported after device is put in I3C Basic mode. In I^2C mode, it is illegal for host to issue this CCC. Table 90 to Table 91 show an example of a single DEVCAP CCC. Table 92 defines the encoding for DEVCAP CCC.

If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W=0 byte in PEC calculation.

12.12.6 DEVCAP CCC (cont'd)

Table 90 — DEVCAP CCC - Direct

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A[1]	
	0xE0 (Direct)								T	
Sr	DevID[6:0]							R=1	A[1]	
	MSB (Each bit defines capability)								T	
	LSB (Each bit defines capability)								T	Sr[2] or P

NOTE 1 The CKD NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
NOTE 2 Repeat Start or Repeat Start with 7'h7E.

Table 91 — DEVCAP CCC - Direct with PEC

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A[1]	
	0xE0 (Direct)								T	
	PEC								T	
Sr	DevID[6:0]							R=1	A[1]	
	MSB (Each bit defines capability)								T	
	LSB (Each bit defines capability)								T	
	PEC								T	Sr[2] or P

NOTE 1 The CKD NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
NOTE 2 Repeat Start or Repeat Start with 7'h7E.

Table 92 — DEVCAP CCC Byte Encoding

Bit	Encoding	Notes
MSB [7]	RFU	Coded as '0'
MSB[6]	RFU	Coded as '0'
MSB[5]	RFU	Coded as '0'
MSB[4]	RFU	Coded as '0'
MSB[3]	RFU	Coded as '0'
MSB[2]	0 = No Support for Timer based Reset 1 = Supports Timer based Reset	Coded as '1'
MSB[1:0]	RFU	Coded as '000'
LSB[7:0]	RFU	Coded as '000'

12.12.7 SETHID CCC

The SETHID CCC is supported only when device is in I^2C mode. In I^2C mode, when host issues CCC, to guarantee that this CCC is registered by the device without any error, the host shall limit the maximum speed operation for this CCC to 1 MHz. In I3C Basic mode, it is illegal for host to issue this CCC. When SETHID CCC is registered by the CKD, it updates with the HID code received by the CKD and it takes in effect at the next Start operation (i.e., after STOP condition). Table 93 shows an example of a single SETHID CCC. As the device is in I^2C mode when SETHID CCC is issued, the PEC function is not supported.

Once CKD receives SETHID CCC and updates its 3-bit HID code after the Stop operation, CKD device only responds to updated 7-bit address. The 4-bit LID code of the CKD device remains as is.

The Host may issue SETHID CCC more than one time.

Table 93 — SETHID CCC - Broadcast

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A	
	0x61 (Broadcast)								T	
	0	0	0	0	HID[2:0]			0	T	P

12.12.8 DEVCTRL CCC

On a typical I3C Basic bus there can be up to 120 devices. For DDR5 DIMM application environment, there are up to 8 SPD5 Hub devices and behind each SPD5 Hub devices, there are 4 local Target devices totaling up to 40 or more devices on I3C Basic bus. For certain operation such as enable or disable functions that are common to all devices (i.e., Packet Error Check), the host must go through one device at a time which takes significant amount of time at initial power up. Further, it requires additional complexity on the host because it must speak different protocol depending on how it may access the device until all devices are configured identically.

To help expedite this configuration operation and to simplify the host complexity, the device supports the DEVCTRL CCC. The DEVCTRL CCC is supported either in I^2C mode or I3C Basic mode of operation. In I^2C mode, when host issues CCC, to guarantee that this CCC is registered by the device without any error, the host shall limit the maximum speed operation for this CCC to 1 MHz. Table 94 to Table 95 show an example of a single DEVCTRL CCC.

If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7’h7E with W=0 byte in PEC calculation.

The host shall pay attention to DEVCTRL CCC. If DEVCTRL CCC is used to access device specific registers (e.g., RegMod = ‘1’), the host shall still follow any device specific register restriction. For example, if device specific register requires STOP operation for device to take in the effect of the setting, the host must also use STOP operation when using DEVCTRL CCC to access device specific register.

12.12.8 DEVCTRL CCC (cont'd)

Table 94 — DEVCTRL CCC - Broadcast

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A[1]	
	0x62 (Broadcast)								T	
	AddrMask[2:0]			StartOffset[1:0]		PEC BL[1:0]		RegMod	T	
	DevID[6:0]							0	T[2]	
	Byte 0 Data Payload								T	
	Byte 1 Data Payload								T	
	Byte 2 Data Payload								T	
	Byte 3 Data Payload								T	Sr[3] or P

NOTE 1 The CKD NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
NOTE 2 An exception is made for DEVCTRL CCC. CKD does report parity error when it determines 7-bit device select code issued by the host does not match with its own device code. If 7-bit device select code does not match but if parity is still valid, the device does not check for parity error in subsequent bytes; ignores the entire packet and waits until STOP or Repeat Start operation.
NOTE 3 Repeat Start or Repeat Start with 7'h7E.

Table 95 — DEVCTRL CCC - Broadcast with PEC[1]

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A[2]	
	0x62 (Broadcast)								T	
	AddrMask[2:0]			StartOffset[1:0]		PEC BL[1:0]		RegMod	T	
	DevID[6:0]							0	T[3]	
	Byte 0 Data Payload								T	
	Byte 1 Data Payload								T	
	Byte 2 Data Payload								T	
	Byte 3 Data Payload								T	
	PEC								T	Sr[4] or P

NOTE 1 DEVCTRL CCC with PEC check is only supported in I3C Basic mode.
NOTE 2 The CKD NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
NOTE 3 An exception is made for DEVCTRL CCC. CKD does report parity error when it determines 7-bit device select code issued by the host does not match with its own device code. The device does not check for PEC as all subsequent bytes are discarded due to parity error. If 7-bit device select code does not match but if parity is still valid, the device does not check for parity error in subsequent bytes; ignores the entire packet and waits until STOP or next Repeat Start operation.
NOTE 4 Repeat Start or Repeat Start with 7'h7E.

12.12.8 DEVCTRL CCC (cont'd)

Table 96 — DEVCTRL CCC Command Definition

Parameter	Definition
AddrMask[2:0]	Broadcast, Unicast or Multicast Command Selection 000 = Unicast Command; CKD device responds if DevID[6:0] field matches with CKD device's own 7-bit address (4-bit LID + 3-bit HID) 011 = Multicast Command; CKD device and possible other device responds if DevID[6:3] field matches with CKD device's own 4-bit LID address 111 = Broadcast Command; All devices responds to this command All other encodings are reserved
StartOffset[1:0]	Only applicable if RegMod = '0' Identifies the starting Byte (Byte 0 or Byte 1 or Byte 2 or Byte 3) for DEVCTRL CCC. Host can start at any Byte (from Byte 0 to Byte 3) and has continuous access to next byte until STOP operation. If Byte 3 is reached, the host is responsible for applying STOP operation. 00 = Byte 0 01 = Byte 1 10 = Byte 2 11 = Byte 3
PEC BL[1:0]	Only applicable if RegMod = '0' and PEC function is enabled. Identifies the burst length just for this DEVCTRL CCC. The device uses the setting in this field to know when the PEC byte is expected after the data bytes. 00 = 1 Byte 01 = 2 Byte 10 = 3 Byte 11 = 4 Byte
RegMod	Identifies if DEVCTRL is going to be used for General Registers as identified in Byte 0 to Byte 3 or device specific address offset register. 0 = Access to General Registers in Byte 0 to Byte 3 (i.e., StartOffset[1:0] = Valid) 1 = Device Specific Offset Address (i.e., StartOffset[1:0] and PECBL[1:0] is a don't care and does not apply). The Host shall NOT use RegMod = '1' with Broadcast Command if there are different types of devices on the I3C Basic bus.
DevID[6:0]	Identifies 7-bit device address. Device responds to DEVCTRL CCC data packet depending on AddrMask[2:0]. If AddrMask[2:0] = '111', DevID[6:0] is a don't care and device always responds. If AddrMask[2:0] = '000', DevID[6:0] must match for device to respond If AddrMask[2:0] = '011', DevID[6:3] must match for device to respond. DevID[2:0] is don't care. For any other codes for AddrMask[2:0], the device always NACKs.

12.12.8 DEVCTRL CCC (cont'd)

Table 97 — DEVCTRL CCC Data Payload Definition

Byte #	Bit #	Function	Definition	Comment
Byte 0	[7]	PEC Enable	0 = Disable 1 = Enable	
	[6]	Parity Dis-able	0 = Enable 1 = Disable	
	[5:2]	RFU	RFU	
	[1]	RSVD	0 = RSVD 1 = RSVD	CKD device always ignores this bit.
	[0]	RFU	RFU	
Byte 1	[7:4]	RFU	RFU	
	[3]	Global and IBI Clear	0 = No Action 1 = Clear All Event and pending IBI[1]	RW28[1:0] are updated
	[2:0]	RFU	RFU	
Byte 2	[7:0]	RFU	RFU	
Byte 3	[7:0]	RFU	RFU	
NOTE 1 After Target device clears the event, the device can still have certain registers set to '1' if the event is still present in which case, the device will generate an IBI again at the next opportunity.				

Table 98 — DEVCTRL CCC Example - Multicast Command to '1001' and '0110' Devices

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A[1]	
	0x62 (Broadcast)								T	
	011			00		00		0	T	
	1001 000							0	T	
	0000 0010								T	
Sr	1	1	1	1	1	1	0	W=0	A[1]	
	0x62 (Broadcast)								T	
	011			00		00		0	T	
	0110 000							0	T	
	0100 0000								T	P
NOTE 1 See Figure 35 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation.										

Table 99 shows an example of DEVCTRL CCC data packet. It assumes that all devices on the bus are already in I3C Basic mode with PEC function disabled and parity function enabled. In this example, the Host uses DEVCTRL CCC as Broadcast command to enable PEC function. The host sends AddrMask = '111' to indicate Broadcast command; StartOffset = '00' to indicate starting Byte 0 and RegMod = '0' to indicates general register. Upon receiving this command, all devices will enable PEC function.

12.12.8 DEVCTRL CCC (cont'd)

Table 99 — DEVCTRL CCC Example - Broadcast Command to all Devices

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A[1]	
	0x62 (Broadcast)								T	
	111			00		00		0	T	
	0000 000							0	T	
	1000 0000								T	P
NOTE 1 See Figure 35 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation.										

Table 100 shows an example of DEVCTRL CCC data packet. It assumes that all devices on the bus are already in I3C Basic mode with PEC function disabled and parity function enabled. In this example, the Host uses DEVCTRL CCC as Unitcast command to enable VR on DIMM5. The host sends AddrMask = '000' to indicate Unicast command; StartOffset = '00' to indicate starting Byte 0 and RegMod = '0' to indicates general register. Upon receiving this command, PMIC on DIMM5 will enable its regulator.

Table 100 — DEVCTRL CCC Example - Unicast Command to PMIC on DIMM5

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A[1]	
	0x62 (Broadcast)								T	
	000			00		00		0	T	
	1001 101							0	T	
	0000 0010								T	P
NOTE 1 See Figure 35 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation.										

12.12.8.1 DEVCTRL CCC Examples - RegMod = '1'

Table 101 shows an example of DEVCTRL CCC data packet for the purpose of configuring device specific address offset register. It assumes that all devices on the bus are already in I3C Basic mode with PEC function enabled and parity function enabled. In this example, the Host sends Multicast command to all devices with 4-bit LID code of '0010' on the I3C Basic bus to write to address offset of 0x1C and 0x1D with data 0xFF and 0x55, respectively, followed by all devices with 4-bit LID of '1001' on the I3C bus to write to address offset of 0x15 with data 0x78.

The PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W=0 byte in PEC calculation.

12.12.8.1 DEVCTRL CCC Examples - RegMod = '1' (cont'd)

Table 101 — DEVCTRL CCC Example - Multicast Command to '0010' and '1001' Devices

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A[1]	
	0x62 (Broadcast)								T	
	011			00		00		1	T	
	0010 000							0	T	
	0001 1100 (address offset 0x1C)								T	
	0010 0000 (CMD field = 2 bytes of data)								T	
	1111 1111 (data)								T	
	0101 0101 (data)								T	
	PEC								T	
Sr	1	1	1	1	1	1	0	W=0	A[1]	
	0x62 (Broadcast)								T	
	011			00		00		1	T	
	1001 000							0	T	
	0001 0101 (address offset 0x15)								T	
	0000 0000 (CMD field = 1 byte of data)								T	
	0111 1000 (data)								T	
	PEC								T	P

NOTE 1 See Figure 35 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation.

Table 102 shows an example of DEVCTRL CCC data packet for the purpose of configuring device specific address offset register. It assumes that all devices on the bus are already in I3C Basic mode with PEC function disabled and parity function enabled. In this example, the Host sends Multicast command to all devices with 4-bit LID code of '1001' on the I3C Basic bus to write to address offset of 0x13 with data 0xFF and it continues to write data 0x01 to the next address.

Table 102 — DEVCTRL CCC Example - Multicast Command to '1001' Devices

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A[1]	
	0x62 (Broadcast)								T	
	011			00		00		1	T	
	1001 000							0	T	
	0001 0011 (address offset 0x13)								T	
	1111 1111 (data)								T	
	0000 0001 (data)								T	P

NOTE 1 See Figure 35 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation.

13 Sideband Interface IO Operation

At power on, by default, the CKD device comes up in legacy I^2C mode of operation with Open Drain IO for its interface. The maximum speed is limited to 1 MHz and supported IO voltage levels are from 1.0 V to 1.8 V.

After power on, the host may put the CKD device in I3C mode of operation. In I3C Basic mode of operation, the maximum speed is limited to 12.5 MHz and supported IO voltage levels are from 1.0 V to 1.8 V.

In I3C Basic mode, the host may drive the SCL clock input of the CKD device using either Push-Pull output driver or using the open-drain output driver. It is expected that for all DDR5 DIMM family environment, the host may always drive the SCL clock input using a Push-Pull output driver.

To support in band interrupt, the CKD device supports dynamic switching between Open Drain mode and Push Pull mode on its SDA bus for various event. The Table 103 describes the different mode of operation by the CKD device for each cycle.

Table 103 — CKD Device Dynamic IO Operation Mode Switching

	Open Drain Mode	Push Pull Mode
START + Device Select Code	Yes	No
START + 7’h7E IBI Header Byte	Yes	No
REPEAT START + Device Select Code	No	Yes
REPEAT START + 7’h7E Header Byte	No	Yes
CCC Bytes (i.e., after 7’h7E+W=0+ACK)	No	Yes
STOP	No	Yes
ACK/NACK Responses	Yes	No
Command, Block Address, Address Operation	No	Yes
Interrupt Request by Target + Device Select Code	Yes	No
IBI Payload	No	Yes
Write Data, T-bit sequence	No	Yes
Read Data, T-bit sequence	No	Yes
PEC, T-bit sequence	No	Yes

13.1 Bus Clear

The CKD device supports the following described Bus Clear feature in I^2C mode only. Any attempt by host to perform I^2C Bus clear on a Target device in I3C mode may result in an active drive bus contention on the SDA data line.

There may be abnormal circumstances when the host abruptly stops clocking SCL while the Target device is in the middle of outputting data for read operation. For these type of events, the SDA data line may appear as stuck low as the device is expecting to receive more clock pulses from the host. Eventually when the host has control of the SCL clock, the host may optionally clear the device that is stuck low on the SDA data line by sending continuous 18 clock pulses without driving the SDA data line followed by STOP operation. The device floats the SDA line within 18 clock pulses and returns to the Idle state. The device is ready for normal new transaction with Start condition.

13.2 Bus Reset

To prevent a malfunctioning device from locking up the I^2C bus or I3C Basic bus, a bus reset mechanism is defined. It uses a timeout mechanism on SCL as shown in Figure to force a device bus reset. All devices on a I^2C or I3C Basic bus reset simultaneously. Bus reset operation works same way regardless of whether device is operating in I^2C or I3C Basic mode.

To guarantee the device resets I^2C bus or I3C Basic bus, the SCL clock input Low time has to be greater than or equal to $t_{TIMEOUT(Max)}$.

The CKD device does not reset I^2C bus or I3C Basic bus if the SCL clock input Low time is less than $t_{TIMEOUT(Min)}$.

If the SCL clock input Low time is between $t_{TIMEOUT(Min)}$ and $t_{TIMEOUT(Max)}$, the CKD device does not guarantee and it may or may not reset the I^2C bus or I3C Basic bus.

When RESET, the CKD device takes following action.

1. Interface and any pending command or transactions are cleared
2. All internal register values are preserved unless noted otherwise in item # 3 below.
3. Sideband mode returns to power-on default conditions as follows: I3C Basic error interrupt disabled, I2C mode enabled, I3C Basic parity checking enabled, I3C Basic PEC checking disabled, Parity and PEC Error Status bits (RW28[1:0]) cleared '00', and Device HID code set to '111'.Device floats the SDA pin such that it gets pulled High by external/other device pullup.
4. Device treats bus reset as STOP operation.

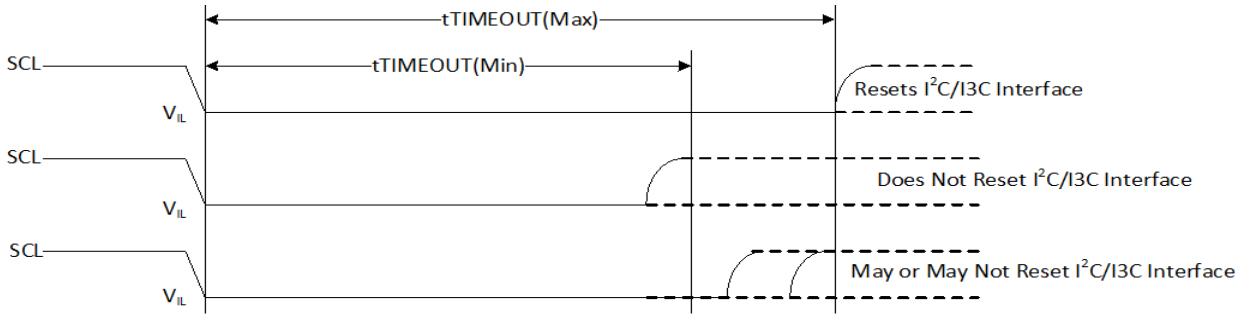


Figure 43 — I^2C or I3C Basic Bus Reset - CKD Device

13.3 Command Truth Table

The command truth table as shown in Table 104 only applies in I3C mode with PEC enabled. In I^2C mode and I3C Basic mode with PEC disabled, the command truth table does not apply.

Table 104 — For I3C Basic Mode only with PEC Enabled - Command Truth Table

CKD Command	Command Name	CMD Code	RW	Address
		2nd Byte Bits [7:5]	2nd Byte Bit [4]	1st Byte Bits [7:0]
Write 1 Byte to Register	W1R	000	0	V
Read 1 Byte from Register	R1R		1	V
Write 2 Byte to Register	W2R	001	0	V
Read 2 Byte from Register	R2R		1	V
Reserved	RSVD	010 to 111	RSVD	RSVD

13.4 AC Timing Definition

13.4.1 I^2C or I3C Basic Bus Timing

The CKD device follow the I^2C or I3C Basic bus timing requirements. Figure 44 through Figure 46 show the timing diagram for Data bus Input and Data Output parameters.

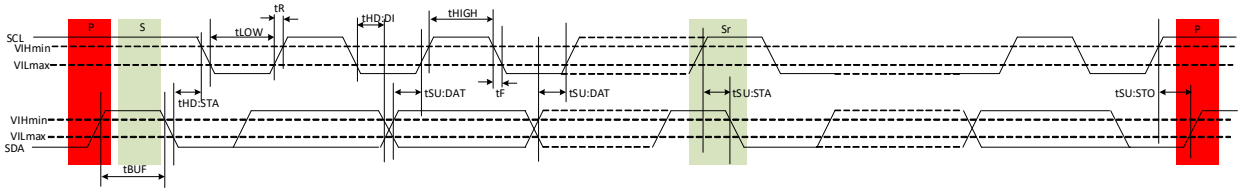


Figure 44 — I^2C or I3C Basic Bus AC Input Timing Parameter Definition

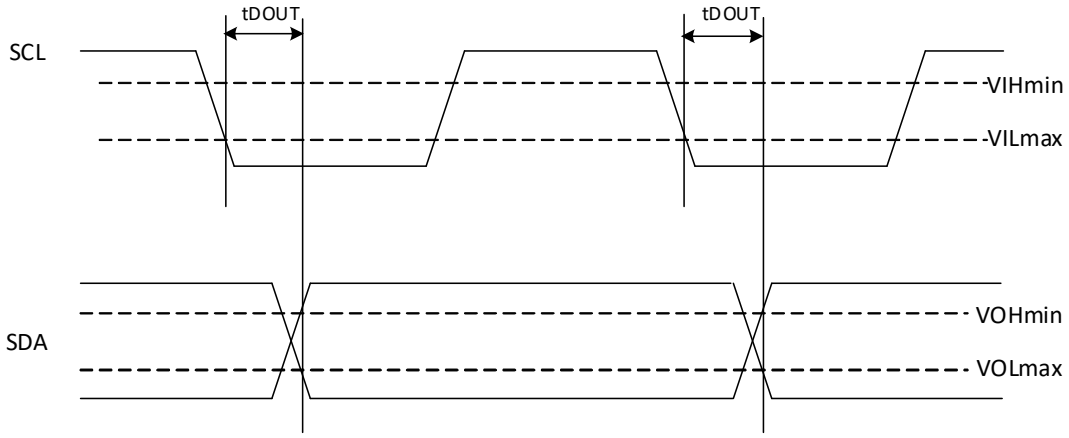


Figure 45 — I3C Basic Bus AC Data Output Timing Parameter Definition

13.4.1 I2C or I3C Basic Bus Timing (cont'd)

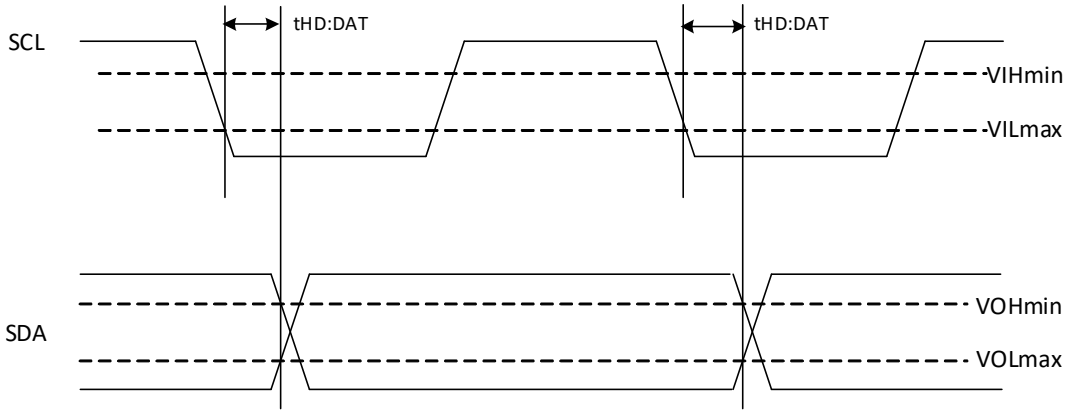


Figure 46 — I²C Bus AC Data Output Timing Parameter Definition

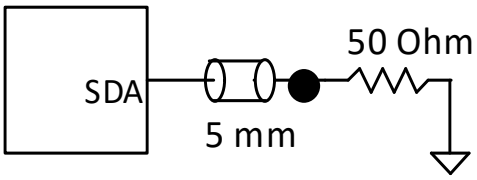


Figure 47 — Output Slew Rate and Output Timing Reference Load

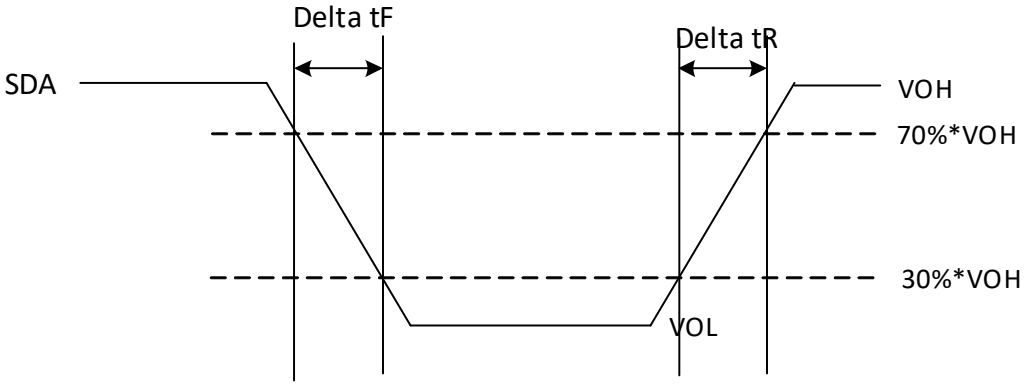


Figure 48 — Output Slew Rate Measurement Points

I2C or I3C Basic Bus Timing (cont'd)

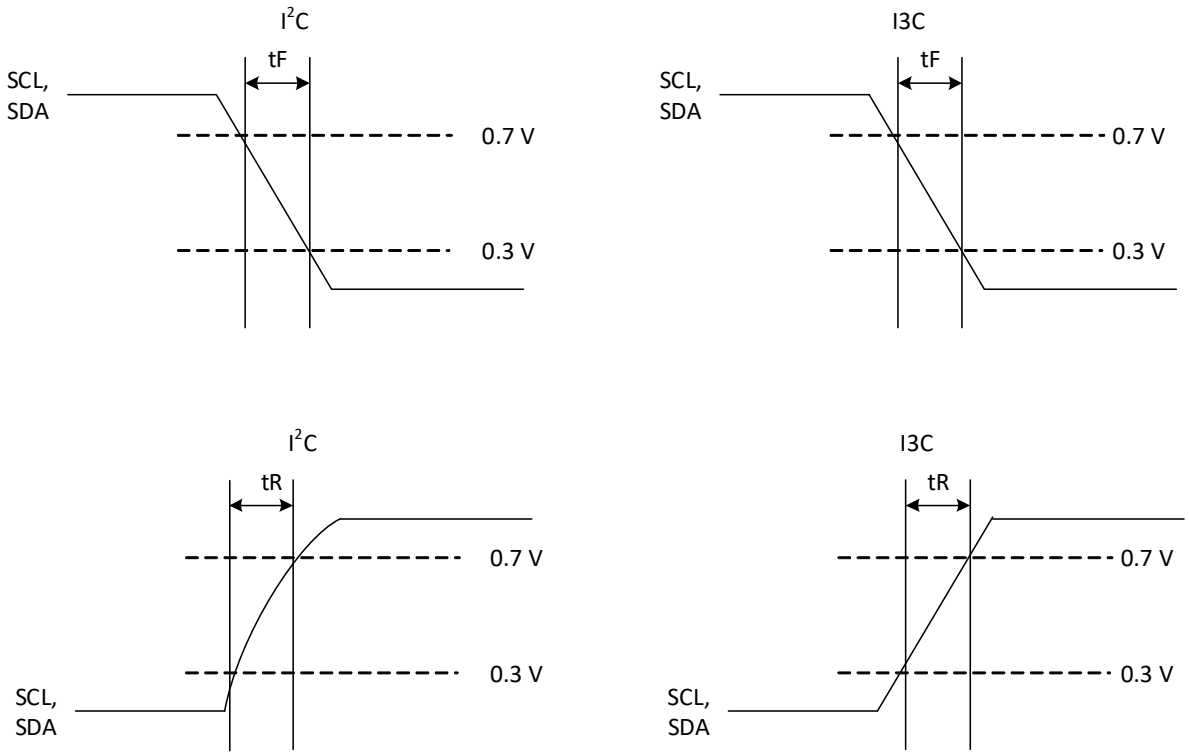


Figure 49 — Rise and Fall Timing Parameter Definition

13.5 Parametric Characteristics

13.5.1 Absolute Maximum Ratings

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 105 — Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V_{DDIO}	Sideband Input Supply Voltage	-0.5	2.1	V
SCL, SDA	SCL, SDA Pins	-0.5	2.1	V

13.5.2 Operating Condition, Measurement Condition, and DC and AC Characteristics

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC Characteristic tables that follow are derived from tests performed under the Measurement Conditions summarized in the relevant tables.

13.5.2 Operating Condition, Measurement Condition, DC and AC Characteristics (cont'd)

Table 106 — DC Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{DDIO}	Sideband Bus Input Supply Voltage for IO[1]	0.95	1.98	V
NOTE 1 CKD must adapt to support either 1.0V or 1.8V typical V_{DDIO}.				

Table 107 — AC Measurement Conditions[1]

Symbol	Parameter	Min	Max	Units
C_L	Load capacitance	40		pF
	Input rise and Fall times - Open Drain	-	TBD	ns
	Input rise and fall times - Push Pull	-	TBD	ns
	Input signal swing levels at V_{DDIO} = 1.0V	0.2 to 0.8		V
	Input and Output timing reference levels at V_{DDIO} = 1.0V	0.3 to 0.7		V
	Input signal swing levels at V_{DDIO} = 1.8V	0.36 to 1.44		V
	Input and Output timing reference levels at V_{DDIO} = 1.8V	0.54 to 1.26		V
NOTE 1 This AC measurement condition (Table 107 and Figure 50) is only for the test purpose in lab.				

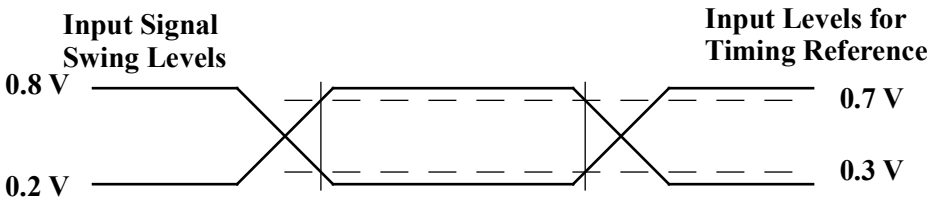


Figure 50 — AC Measurement Waveform

Table 108 — Input Parameters

Symbol	Parameter[1,2]	Test Condition	Min	Max	Units
C_{IN}	Input capacitance (SDA, SCL)	--	--	5	pF
t_{SP}	Pulse width of spikes which must be suppressed by the input filter in I^2C mode.	Single glitch, f ≤ 100 KHz	--	--	ns
		Single glitch, f > 100 KHz	0	50	
NOTE 1 T_A = 25 °C, f = 400 kHz NOTE 2 Verified by design and characterization, not necessarily tested on all devices					

13.5.2 Operating Condition, Measurement Condition, DC and AC Characteristics (cont'd)

Table 109 — Output Ron Spec

Symbol	Parameter	Condition	Min	Max	Units	Notes
$R_{on_1.0}$	SDA, Output Pullup and Pulldown Driver Impedance	VDDIO = 1.0 V	10	45	Ohm	1
$R_{on_1.8}$	SDA, Output Pullup and Pulldown Driver Impedance	VDDIO = 1.8V	5	35	Ohm	1
NOTE 1 Pulldown Ron = Vout/Iout; Pullup Ron = (VDDIO - Vout)/Iout						

Table 110 — DC Characteristics

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input leakage current (SCL, SDA)	$V_{IN} = V_{SS}$ or V_{DDIO}	--	±5	µA
I_{LO}	Output leakage current	$V_{OUT} = V_{SS}$ or V_{DDIO}, SDA in Hi-Z	--	±5	µA
I_{DDIO}	Supply current	V_{DDIO} = 1.0 V, f_C = 12.5 MHz (rise/fall time < 5 ns)	--	5	mA
V_{IL}	Input LOW voltage (SCL, SDA)	See Note 1	-0.35	0.3 x V_{DDIO}	V
V_{IH}	Input HIGH voltage (SCL, SDA)	See Note 2	0.7 x V_{DDIO}	V_{DDIO} + 0.3	V
V_{OL}	Output LOW voltage (SDA)	3-mA sink current	--	0.3	V
V_{OH}	Output HIGH voltage (SDA)	3-mA source current	V_{DDIO} - 0.3	--	V
I_{OL}	LOW-level output current	V_{OL} = 0.3 V	3	-	mA
I_{OH}	HIGH-level output current	$V_{OH} = V_{DDIO}$ - 0.3	-	-3	mA
Slew_Rate_1.0	Output Slew Rate (SDA)	V_{DDIO} = 1.0 V See Note 3	0.1	1.0	V/ns
Slew_Rate_1.8	Output Slew Rate (SDA)	V_{DDIO} = 1.8 V See Note 3	0.25	5.0	V/ns

NOTE 1 Undershoot might occur. It should be limited by the Absolute Maximum DC Ratings.
NOTE 2 Overshoot might occur. It should be limited by Absolute Maximum DC Ratings
NOTE 3 Output slew rate is guaranteed by design and/or characterization. The output slew rate reference load is shown in Figure 47 and Figure 48 shows the timing measurement points.

13.5.2 Operating Condition, Measurement Condition, DC and AC Characteristics (cont'd)

Table 111 — AC Characteristics

Symbol	Parameter	I^2C Mode - Open Drain		I3C Basic Push-Pull[1]		Units	Notes
		Min	Max	Min	Max		
f_{SCL}	Clock frequency	0.01	1	0	12.5	MHz	
t_{HIGH}	Clock pulse width high time	260	--	35	--	ns	
t_{LOW}	Clock pulse width low time	500	--	35	--	ns	
$t_{TIMEOUT}$	Detect clock low timeout	10	50	10	50	ms	
t_R	SDA rise time	--	120	--	5	ns	2,3
t_F	SDA fall time	--	120	--	5	ns	2,3
$t_{SU:DAT}$	Data in setup time	50	--	8	--	ns	2
$t_{HD:DI}$	Data in hold time	0	--	3	--	ns	2
$t_{SU:STA}$	Start condition setup time	260	--	12	--	ns	2
$t_{HD:STA}$	Start condition hold time	260	--	30	--	ns	2
$t_{SU:STO}$	Stop condition setup time	260	--	12	--	ns	2
t_{BUF}	Time between Stop Condition and next Start Condition	500	--	500	--	ns	2,4
t_{AVAL}	Bus Available time (no edges seen on SDA and SCL)	-	-	1	--	µs	
t_{IBI_Issue}	Time to issue IBI after an event is detected when Bus is available	-	-	-	15	µs	
$t_{CLR_I3C_CMD_Delay}$	Time from Clear Register Status to any I3C operation with Start condition to avoid IBI generation; PEC disabled	-	-	4	-	µs	
	Time from Clear Register Status to any I3C operation with Start condition to avoid IBI generation; PEC enabled	-	-	15	-	µs	
$t_{HD:DAT}$	SCL Falling Clock In to SDA Data Out Hold Time	0.5	350	N/A	N/A	ns	5
t_{DOUT}	SCL Falling Clock In to SDA Valid Data Out Time	N/A	N/A	0.5	12	ns	6
t_{DOFFT}	SCL Rising Clock In to SDA Output Off	N/A	N/A	0.5	12	ns	7
t_{DOFFC}	SCL Rising Clock In to Controller SDA Output Off	N/A	N/A	0.5	t_{HIGH}	ns	8
$t_{CL_r_DAT_f}$	SCL Rising Clock In to Controller Driving SDA Signal Low	N/A	N/A	40	-	ns	9
$t_{DEVCTRLCCC_PEC_DIS}$	DEVCTRL CCC Followed by DEVCTRL CCC or Register Read/ Write Command Delay	3	-	3	-	µs	10, 11, 12
$t_{WR_RD_DELAY_PEC_EN}$	Register Write Command Followed by Register Read Command Delay in PEC Enabled Mode	N/A	N/A	8	-	µs	13, 14, 15

13.5.2 Operating Condition, Measurement Condition, DC and AC Characteristics (cont'd)

Table 111 — AC Characteristics (cont'd)

Symbol	Parameter	I^2C Mode - Open Drain		I3C Basic Push-Pull[1]		Units	Notes
		Min	Max	Min	Max		
$t_{I2C_CCC_Update_Delay}$	SETHID CCC or SETAASA CCC to any other CCC or Read/Write Command delay	2.5	-	-	-	µs	
$t_{I3C_CCC_Update_Delay}$	RSTDAA CCC or ENEC CCC or DISEC CCC to any other CCC or Read/Write Command Delay	N/A	N/A	2.5	-	µs	
t_{CCC_Delay}	Any CCC to RSTDAA CCC delay	N/A	N/A	2.5	-	µs	

NOTE 1 I3C mode with Open Drain operation follows timing values as shown in I^2C Mode - Open Drain column.
NOTE 2 See Figure 44 for input timing parameter definition.
NOTE 3 See Figure 49 for voltage threshold definition for rise and fall times.
NOTE 4 If PEC is enabled, $t_{WR_RD_DELAY_PEC_EN}$ timing parameter also applies.
NOTE 5 See Figure 46 for output timing parameter definition
NOTE 6 The CKD device must be configured in I3C mode to guarantee t_{DOUT} value. See Figure 45 for data output timing parameter definition. See Figure 47 for output timing parameter measurement reference load.
NOTE 7 The CKD device must be configured in I3C mode to guarantee t_{DOFFT} value. See Figure 47 for output timing parameter measurement reference load.
NOTE 8 The CKD device must be configured in I3C mode. The Host guarantees t_{DOFFC} value. See Figure 47 for output timing parameter measurement reference load.
NOTE 9 See Figure .
NOTE 10 From STOP condition of DEVCTRL CCC to START condition for Register Read or Register Write Command Data Packet delay.
NOTE 11 The device sends NACK if Host does not satisfy $t_{DEVCTRLCCC_DELAY_PEC_DIS}$ timing parameter.
NOTE 12 This timing parameter restriction is only applicable when PEC function is disabled in CKD. If PEC is enabled, this timing parameter does not apply.
NOTE 13 From STOP condition for Register Write Command Data Packet to START condition for Register Read Command Data Packet delay.
NOTE 14 This timing parameter restriction is only applicable when PEC function is enabled in CKD. If PEC is disabled, this timing parameter does not apply.
NOTE 15 The CKD sends NACK if Host does not satisfy $t_{WR_RD_DELAY_PEC_EN}$ timing parameter.

14 Reference to other Applicable JEDEC Standards and Publications

- JEP95, JEDEC Registered and Standard Outlines for Solid State and Related Products.
- JEP104, Reference Guide to Letter Symbols for Semiconductor Devices.
- JESD21-C, Configuration for Solid State Memories.
- JESD8-11A, Definition of wide range non-terminated logic.
- JESD79-5, DDR5 SDRAM Specification.
- MO-TBD, Package Mechanical Outline.
- I3C Basic, Specification for I3C Basic Version 1.0 – 19 July 2018.
- JESD403-1, Specification for JEDEC Module SidebandBus.
- JS-001-2017, Joint JEDEC/ESDA Standard for Electrostatic Discharge Sensitivity Test – Human Body Model (HBM) – Component Level.
- JS-002-2018, ANSI/ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing – Charged Device Model (CDM) – Device Level.

Annex A — (Informative) Differences between Revisions

A.1 Differences between JESD82-531A and JESD82-531 (dated May 2023)

- Replaced all instances of "CK01" with "CKD01" to follow the new JEDEC name. This replacement includes a number of tables
- Replaced all instances of "DDR5CK01" with "DDR5CKD01" to follow the new JEDEC name. This replacement includes a number of tables
- Modified Table numbers 34, 38, 39, 45, and 50
- Modified Figure number 1

A.2 Differences between JESD82-531A.01 and JESD82-531A (dated January 2024)

- Corrected errors in Table numbers 34, 38, 39, 45, and 50
- Corrected typographical error in the label of Figure 32 (DDR5CK01 to DDR5CKD01)
- Changed 2nd sentence in clause 12.2 from DDR5CK to DDR5CKD01

Standard Improvement Form **JEDEC Standard JESD82-531A.01**

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

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☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

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